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NORMALLY-OFF GAAS FET MONOLITHIC TECHNOLOGY.(U)
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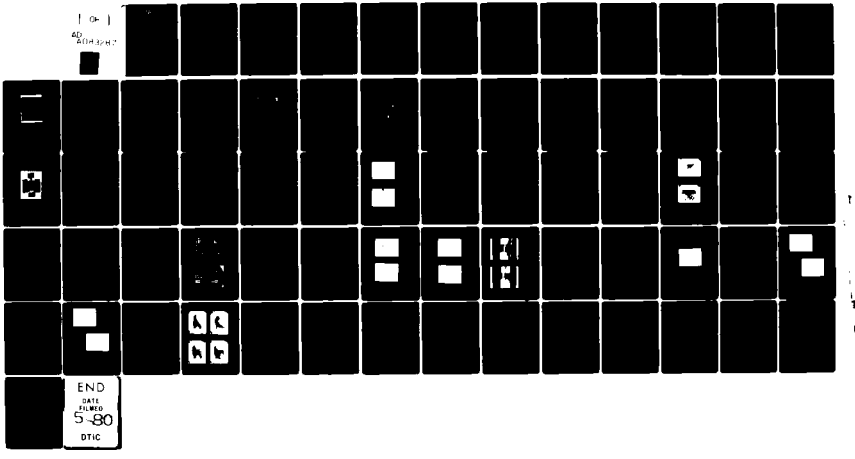

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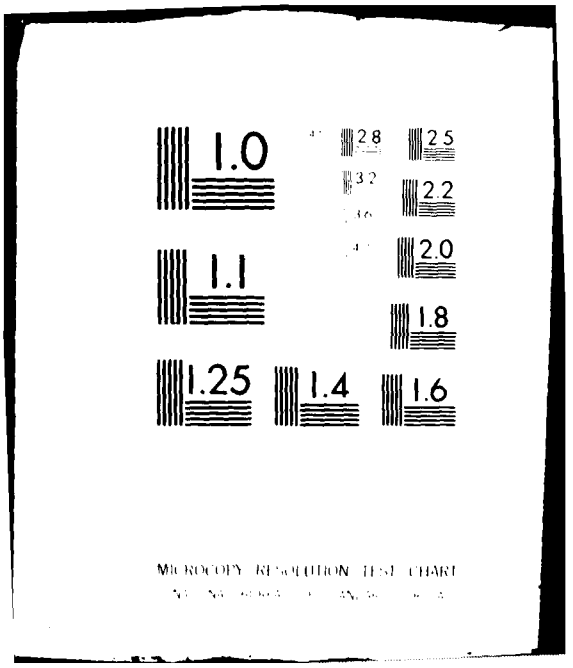
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NORMALLY-OFF GaAs FET MONOLITHIC TECHNOLOGY

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The purpose of this work is to develop technology to improve performance of $Al_{.5}Ga_{.5}As$ gate FETs for high-speed logic application. Normally-off and normally-on heterojunction gate FETs, fabricated from layers grown by organometallic and vapor-phase epitaxy, are studied and are compared with metal gate FETs using microwave and large-signal switching response as criteria.

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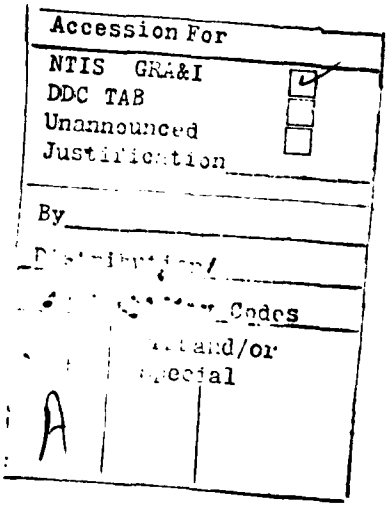

SUMMARY

$Al_{.5}Ga_{.5}As$ gate heterojunction field-effect transistors (HJFETs) have been fabricated using organometallic (OM) epitaxy and tested. Growth of the FET active layer on an undoped buffer layer has been shown to produce less velocity degradation at the channel-substrate interface than if the active layer is grown directly on a Cr-doped substrate. HJFETs have been fabricated by growing the p-$Al_{.5}Ga_{.5}As$ and p^+-GaAs OM gate layers on mesa-etched vapor-phase epitaxy (VPE) active layers and also by growing all three layers by OM epitaxy. Electrical measurements on normally-on and normally-off HJFETs indicated a problem at the p-$Al_{.5}Ga_{.5}As$/n-GaAs interface, later confirmed by the finding of significant amounts of oxygen in the $Al_{.5}Ga_{.5}As$.

Microwave small signal and large signal switching measurements were made on HJFETs with 2x300 micron gates and on Schottky barrier FETs (SBFETs) with 1x200 micron Al gates intended to simulate normally-off HJFETs. Circuit models were derived from the small-signal measurements and gate propagation delays were derived from the switching measurements. A 2-micron gate normally-on HJFET had 47 psec gate propagation delay while a 1-micron gate SBFET (simulated normally-off HJFET) had 27 psec gate propagation delay.

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1. INTRODUCTION

Previous efforts to fabricate p-$Al_{.5}Ga_{.5}As$/n-GaAs heterojunction gate field-effect transistors (HJFETs)[1,2] used gate layers grown by liquid-phase epitaxy (LPE). A pH 7.05 superoxol solution, requiring constant pH monitoring, was used to etch the p^+-GaAs gate cap layer. HF was used to etch the $Al_{.5}Ga_{.5}As$ to provide the undercutting needed for self-alignment. FET characteristics indicated a fairly good p-n heterojunction, probably because of the slight meltback of the n-GaAs active layer during LPE. However, there were some problems with uniformity and minimum thickness of LPE gate layers. Other measurements indicated that substantial carrier velocity degradation occurred near the interface between the n-GaAs active layer and the semi-insulating substrate.

In the present work, process technology for HJFETs and HJFET ring oscillators has been substantially improved. These transistors were fabricated by growing the active layer on an undoped GaAs vapor-phase epitaxy buffer layer so that velocity degradation at the channel-substrate interface is no longer a problem. P-type gate layers of $Al_{.5}Ga_{.5}As$ (henceforth, AlGaAs) and GaAs were grown by organometallic (OM) epitaxy, which offers the advantages of thinner and more uniform epi than liquid-phase epitaxy, better surfaces, and the possibility of higher dopings where desired. The p^+-GaAs gate etch was done efficiently with a citric acid solution that is more stable than a superoxol pH 7.05 solution.

Some Al-gate Schottky-barrier FETs (SBFETs) on vapor-phase epitaxy (VPE) active layers having about -0.5V pinch-off (0.13 micron thick and $1 \times 10^{17}/cm^3$ donor concentration)

were fabricated in order to simulate the normally-off HJFET with its 1.4V built-in gate voltage. DC measurements revealed that growing the active layer on a buffer layer solved the velocity degradation problem, while fast pulse measurements showed that 27 psec gate propagation delay time should be possible for the normally-off HJFET.

Normally-on (N-on) and normally-off (N-off) HJFETs were fabricated by OM epitaxy of the gate layers on a mesa-etched VPE active layer. Some N-on VPE/OM HJFETs with 2x300 micron gates were found to have 47 psec gate propagation delay. N-off VPE/OM HJFETs were also made but had +1V to +4V threshold voltage, indicating a problem at the AlGaAs/GaAs interface. Other evidence of interfacial traps was seen with the N-on HJFETs.

HJFETs were also fabricated by growing the active FET layer and the gate layers by OM epitaxy (all-OM HJFETs). Since all three layers were grown at once and the mesa etch then leaves the gate layers on top of the mesa only, an oxide protection on the side of the mesa is necessary before metallization. N-on HJFETs fabricated in this way also showed evidence of interfacial traps even though the heterojunction was grown in the OM reactor. Oxygen in the OM-grown AlGaAs was later found to be the reason.

Since this technology is aimed toward high-speed normally-off logic, efforts to use the HJFET technology with a ring oscillator mask set were undertaken. The ring oscillator work helped to improve some HJFET processes and ensured that a ring oscillator test of N-off HJFET logic can be done as soon as satisfactory N-off HJFETs can be fabricated from oxygen-free OM material.

2. INVESTIGATION AND DISCUSSION

2.1 Organometallic Vapor Phase Epitaxial Growth of Heterojunction FETs

2.1.1 OM-VPE Growth

Interest in organometallic-sourced vapor phase epitaxy (OM) for the growth of III-V semiconducting compounds has increased considerably since the utility of the process was demonstrated in 1968.[3,4] Organometallic-sourced VPE has several advantages over other growth techniques such as liquid-phase epitaxy (LPE), molecular beam epitaxy (MBE) and conventional chloride transport vapor-phase epitaxy. The growth of single crystal layers of AlGaAs by conventional VPE, for example, is difficult owing to unfavorable thermodynamic constraints.[5] With OM, however, AlGaAs grows relatively easily. Growing an alloy of specific composition, using OM is simplified because of the close correspondence between the vapor and solid phase composition. Organometallic grown materials normally exhibit superior surface morphology and better uniformity of the layer composition, thickness and doping levels as compared to LPE grown materials. The organometallic sourced process utilizes a much simpler apparatus than MBE without giving up some of the advantages of MBE, such as the capability of growing extremely sharp heterojunctions.

The system used in this work (Fig. 1) was a horizontal cold wall reactor with an rf-induction heated graphite susceptor. The system consists of three main portions: the chemical sources, mass flow controllers and plumbing to

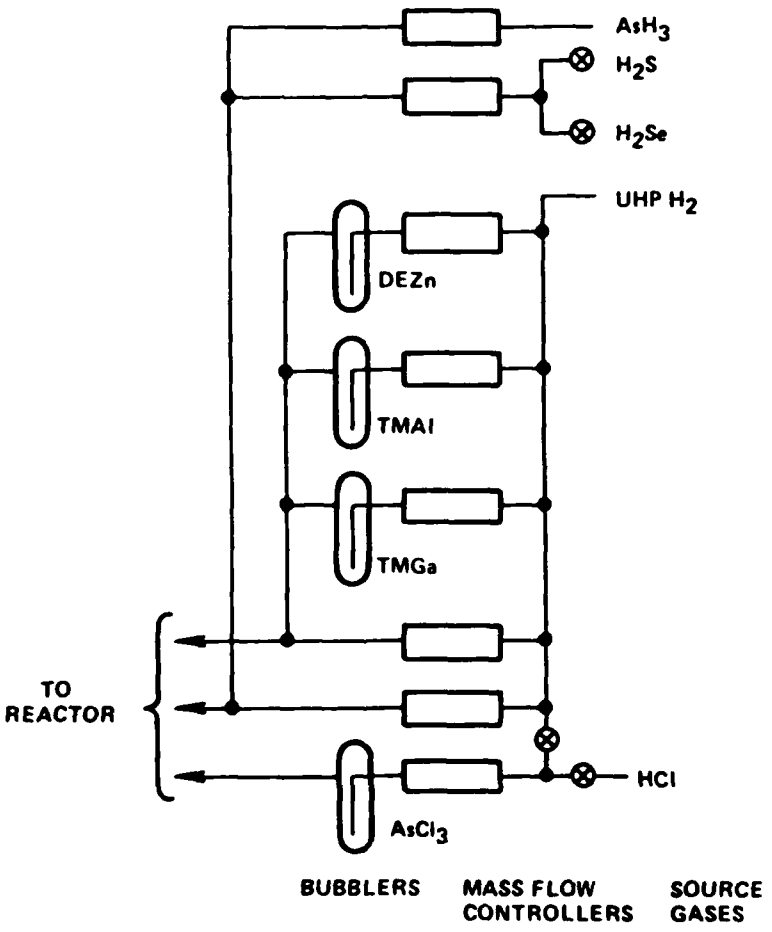


Fig. 1 Schematic diagram of organometallic epitaxy system.

regulate and transport the chemicals, and the reactor. Trimethylgallium (TMGa) and trimethylaluminum (TMAl) are used as the Group III sources while arsine ((10%) in H_2) is used as the Group V source. Diethylzinc (DEZn) and hydrogen sulfide (400 ppm H_2S in H_2) are used as p- and n-type dopants respectively. The metal alkyls (TMAl, TMGa, and DEZn) exist as liquids at ambient conditions and are extremely reactive in the presence of air or water. These materials are contained in stainless bubblers through which a stream of purified hydrogen is passed to transport the chemicals to the growth zone. Arsenic trichloride can be used for in situ etches of the substrates prior to growth.

In a typical growth, the GaAs wafer is cleaned using standard procedures and then placed on the graphite susceptor and loaded into the reactor. After a hydrogen purge of 30 minutes, the rf generator is started and the water is warmed to the desired temperature. During this procedure arsine is flowed through the reactor to retard substrate decomposition. After the temperature is stabilized, the Group III reactants and desired dopants are flowed into the reactor and the growth takes place.

2.1.2 Results

Gallium arsenide can be grown over a wide range of temperatures and input fluxes. The epitaxial layers grown in this work were grown with a Group III to Group V ratio of 10. Typical mole fractions for TMGa and AsH_3 in the growth zone were 1.3×10^{-4} and 1.3×10^{-3}, respectively with a total hydrogen flow of 9.5 slpm. These input fluxes resulted in a growth rate of 0.05 microns/minute at a growth temperature of 730°C.

Single crystal layers of $Al_{.5}Ga_{.5}As$ were also grown at 730°C with total Group III mole fraction of 1.3×10^{-4} and a Group V mole fraction of 1.3×10^{-3}. Since the vapor phase ratio of TMAl and TMGa closely follows the Al/Ga ratio in the crystal, equal fluxes of TMAl and TMGa were introduced into the growth zone. AlGaAs growth was investigated both with and without HCl (introduced as HCl 2% in hydrogen) present in the system. Low HCl fluxes (6.5×10^{-5} mole fraction) gave superior surface morphologies.

Abrupt heterojunctions are essential in HJFET devices. Therefore, a preliminary profiling of an OM-grown heterojunction was performed using a Varian UHV ion-milling Auger electron analysis system. The sample, which contained a step composition change from $Al_{.6}Ga_{.4}As$ to GaAs cap layer, exhibited a 10 to 90% transition region of 42 Å. This is a very abrupt transition considering some broadening of the transition probably resulted from the ~1000 Å of GaAs that was sputtered through to get to the surface. Furthermore, the Al Auger peak that was monitored was centered at 1432 eV. Auger electrons at this energy have escape lengths of ~20 Å and are not the optimum electrons to monitor. This result, however, demonstrates that extremely sharp heterojunctions can be achieved by OM.

Undoped GaAs layers were n-type and exhibited $N_d + N_a$ values as low as $1.3 \times 10^{14} cm^{-3}$ with an associated mobility at 77°K of 111,500 cm^2/V-sec. Gallium arsenide epitaxial layers can be intentionally n or p doped to levels in the $10^{19} cm^{-3}$ region by regulating the input fluxes of the dopants (H_2S or DEZn). A DEZn mole fraction on the order of 10^{-5}, for example, resulted in a doping level of $5 \times 10^{18} cm^{-3}$

in GaAs. The highest p-type doping levels attained in AlGaAs were in the $10^{18}cm^{-3}$ region, which is an order of magnitude lower than the comparable doping levels attainable in GaAs. However, all these measurements were made for the $Al_{.9}Ga_{.1}As$ solar cell layers.

Devices were grown by a hybrid technique as well as entirely by organometallic VPE. The all OM structures consisted of a sulfur doped GaAs active layer which was grown directly on a VPE buffer layer followed by the AlGaAs (Zn doped) and GaAs (Zn doped) cap. The hybrid growth consisted of OM-grown AlGaAs and GaAs layers which were deposited on a chloride transport VPE-grown mesa-etched active layer.

AlGaAs and GaAs gate layers, each about 3300 Å thick, can clearly be seen in Fig. 2, a scanning electron microscope (SEM) photograph of a cleaved HJFET gate after selective etching. The gate etch procedure will be described later.

2.2 Improvement of Active Layer Carrier Velocity Profile

Earlier work on HJFETs[1,2] showed that significant degradation of carrier velocity in the n-GaAs active layer occurs when the active layer is grown on a Cr-doped substrate. A profile of the carrier velocity v_s can be obtained from a plot of I_{DS} versus the square root of the effective gate bias.[2] Figure 3 shows two carrier velocity profiles in the form of v_s versus distance from the channel-substrate interface. It should be noted that the exact position of the interface and the scaling of v_s are somewhat arbitrary with this measurement technique. Curve (a), reproduced from

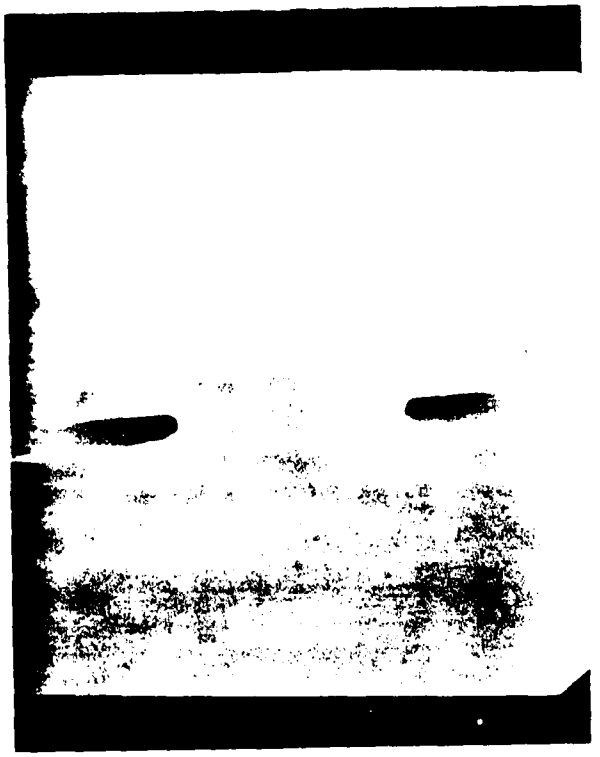


Fig. 2 15,200X SEM photo of cleaved HJFET gates. Gate cap is about 4.6 microns wide, AlGaAs and GaAs layers each about 3300 Å thick.

Refs. 1 and 2, is a profile for a normally-on HJFET and is typical of active layers grown directly on a Cr-doped substrate. Carrier velocity begins to decline a substantial distance from the interface.

One of the first tasks undertaken in this work was to investigate the carrier velocity profile for an active layer grown on a buffer layer, in the hope that the improved channel-substrate interface would confine velocity degradation to a narrower region. Curve (b) in Fig. 3 shows a velocity profile for such a layer, taken from measurements on a normally-on Schottky-barrier FET with VPE active layer grown on a 3-micron VPE buffer layer. Clearly the improved channel-substrate interface relieves the velocity degradation problem considerably, cutting the width of the velocity-degraded part of the channel from 500 Å to 200 Å. This should mean substantially improved performance for normally-off heterojunction FETs, which in switching applications make heavy use of the channel near the interface.

2.3 Fabrication Techniques

2.3.1 VPE/OM HJFETs

Earlier work in this laboratory on HJFETs [1, 2] concentrated on a device built by growing liquid phase epitaxy (LPE) p-AlGaAs and p^+-GaAs gate layers on top of a mesa-etched vapor-phase epitaxy (VPE) n-GaAs active layer. After selective etching of the gate layers, a self-aligned source-gate-drain AuGe/Ni/Au metallization is done, then gold bonding pads are evaporated. The resulting heterojunction FET is shown in Fig. 4. Similar devices were

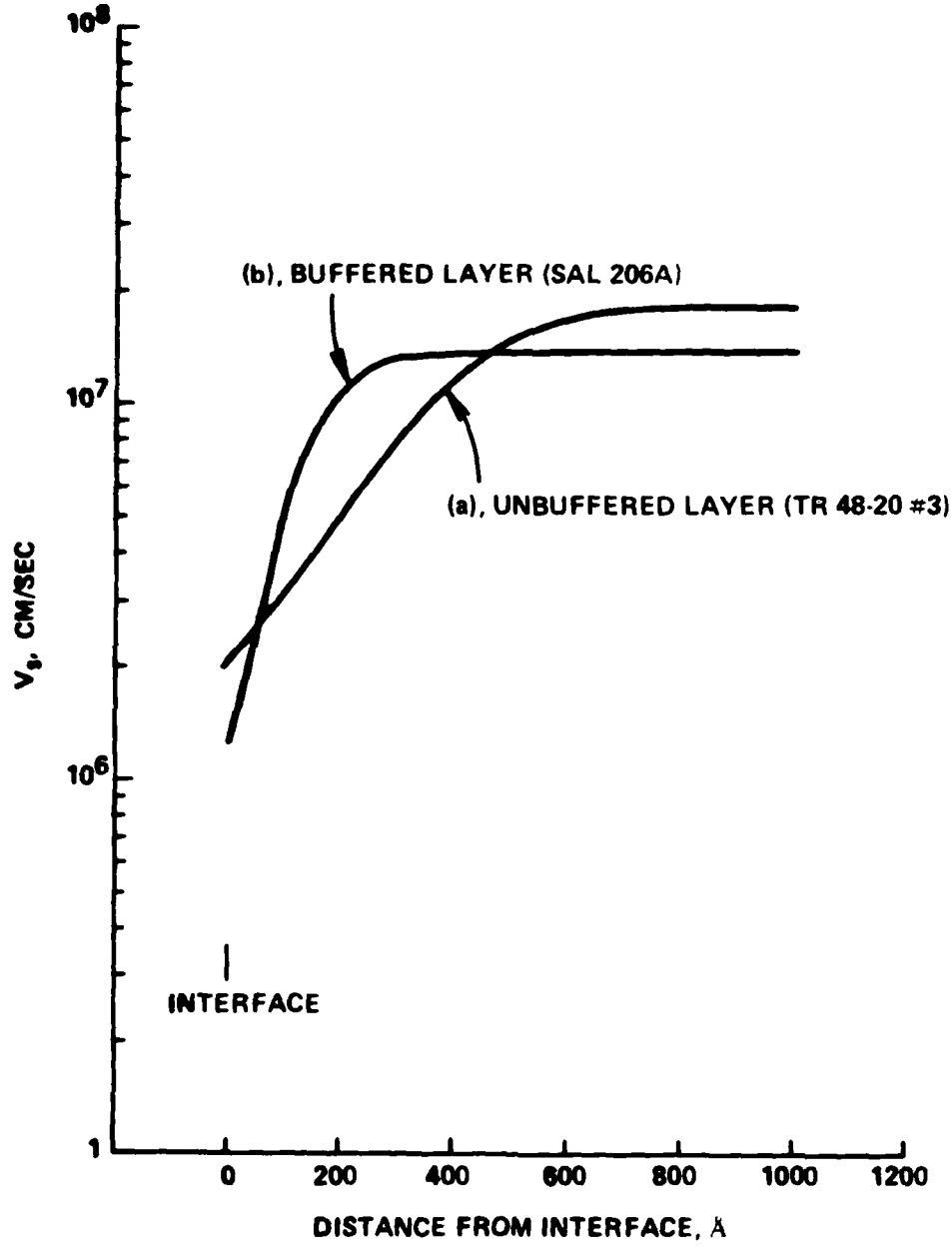


Fig. 3 SATURATION VELOCITY VS. DISTANCE FROM INTERFACE

fabricated in this work, using organometallic (OM) epitaxy for the gate layers. OM epitaxy offers the advantages of thinner and more uniform epi, better surface morphology, lower temperature growth, and no meltback of the active layer as with LPE. Also it was hoped that OM would give more reproducible layers than LPE.

The fabrication steps for the VPE/OM HJFETs are shown in Fig. 5. First a VPE active layer is grown on a buffer layer, the latter being for the sake of the carrier velocity profile, as discussed in Section 2.2. Before the mesa etch determines the direction of the gates, it is necessary to find the (011) direction on the GaAs wafer by studying elongated etch pits formed during an etch in 3:1:15 ($NH_4OH:H_2O_2:H_2O$). V-type gates (tapering to a short gate width, see Fig. 6) will result when the gates are properly oriented with respect to (011). Reference 1 discusses this procedure at length but contradicts itself concerning the proper orientation of the gates with respect to the etch pits. In this work it was often difficult to tell if the gates were V or inverted-V because the AlGaAs was perhaps 2500 Å thick and 2 or 3 microns wide. Gates were oriented both parallel and perpendicular to the elongated etch pits and it appeared that V-type gates developed when the 150 micron length of the gate was oriented parallel to the elongated etch pits.

The mesas are then defined with 3:1:1 ($H_2O:HF:H_2O_2$) or 3:1:15 ($NH_4OH:H_2O_2:H_2O$) as discussed in Ref. 1. After the OM growth of the p-AlGaAs (about $1 \times 10^{18}/cm^3$ Zn doping) and p^+-GaAs (about $1 \times 10^{19}/cm^3$ Zn doping) layers, about 0.3 micron each, the wafer is ready for gate definition.

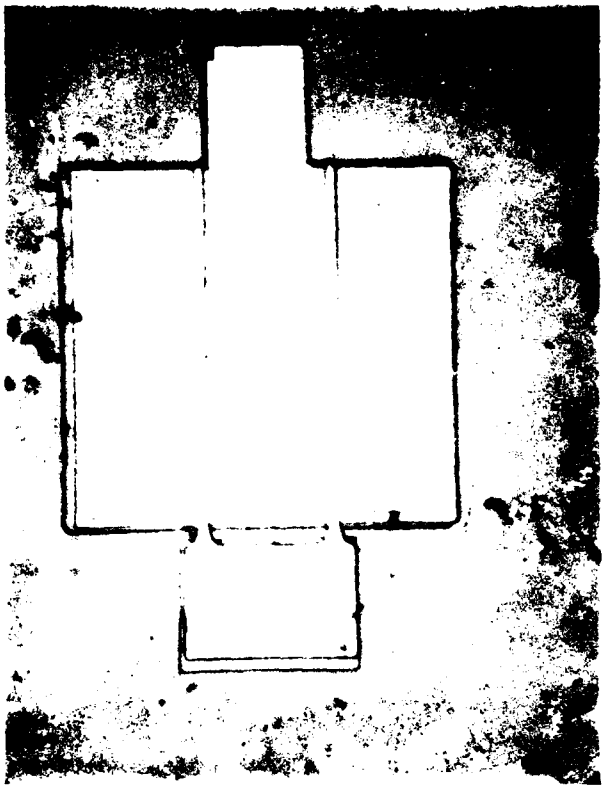


Fig. 4 Top view of completed HJFET.

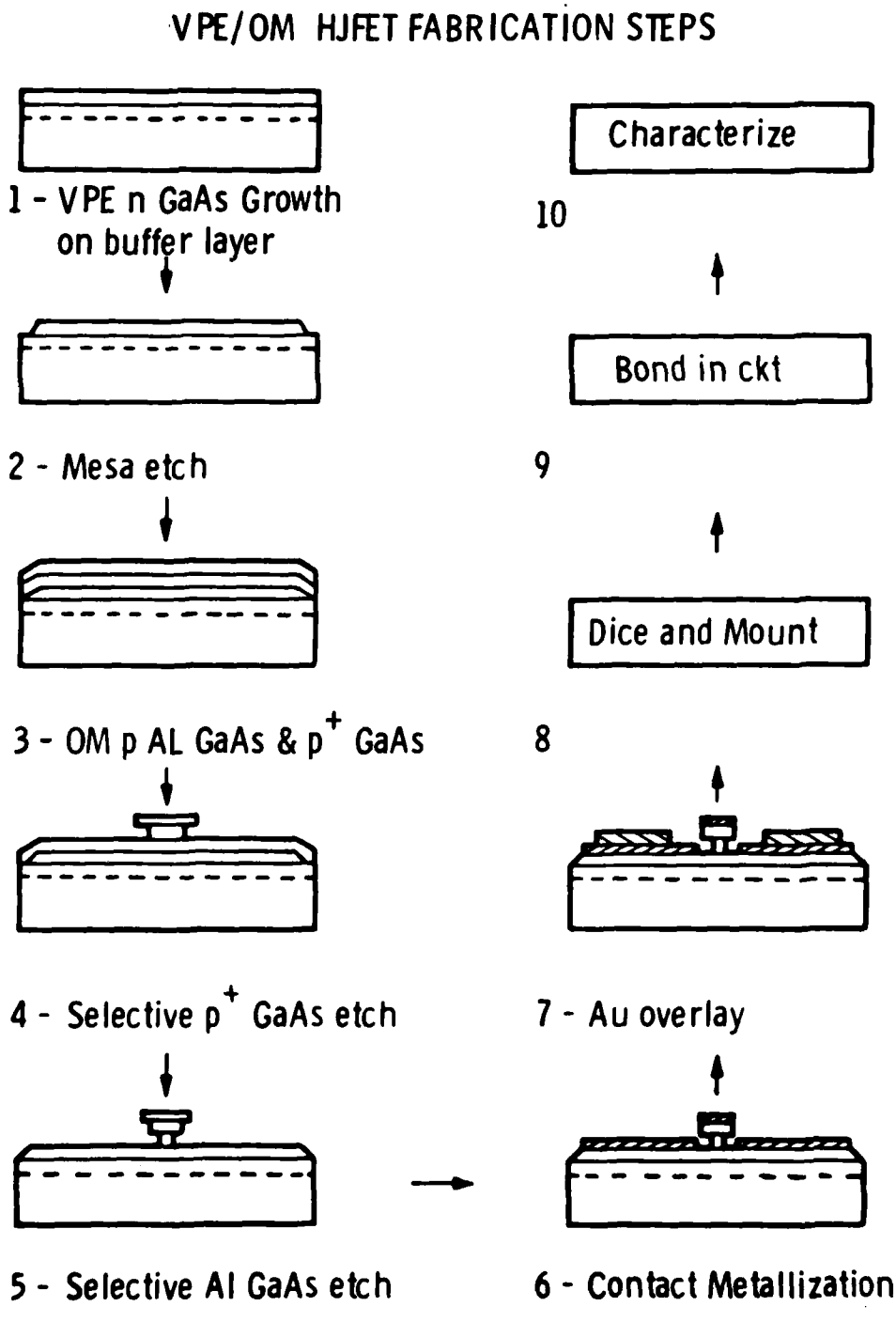


Fig. 5 **Fabrication of heterojunction FET with OM gate layers on VPE active layer.**

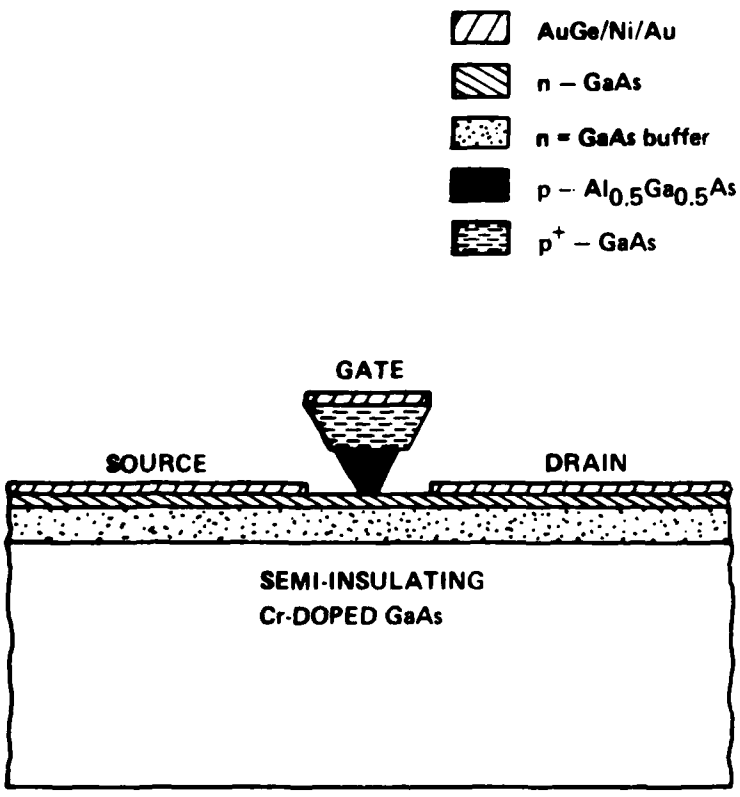


Fig. 6 Schematic diagram of HJFET aligned along the (011) direction.

The 5x300 micron gate pattern is then defined using Shipley AZ 1350J positive photoresist, or Kodak 747 negative photoresist. The p^+-GaAs cap layer is selectively etched in a k=10 citric acid:H_2O_2 solution at room temperature.[6] If negative photoresist is deposited, a brief plasma etch ("descum") must precede the gate etch or else a thick bluish haze, nearly impossible to remove, will develop over the wafer in the citric acid etch. The k=10 citric acid solution etches GaAs at a nominal rate of 40 Å/sec and so 2-2.5 minutes ensures that the layer is etched and the gate slightly undercuts the photoresist.

In previous studies[1, 2] a pH 7.05 superoxol etch was used for the p^+-GaAs selective etch. While it performed adequately, this etch was found to age rapidly and it needed almost continual monitoring with a pH meter. Like the superoxol etch, the citric acid etch[6] was a good preferential etch for GaAs which does not erode photoresist. But the citric acid etch also is easy to prepare, needs no monitoring, and does not age noticeably for at least two or three days. Using citric acid for the p^+-GaAs cap layer etch allowed the gate etch step to be performed much more rapidly than before.

In previous HJFET work[1, 2] the preferential GaAs cap etch was often allowed to reduce the cap layer to a width of 1-2 microns, using a 5-micron wide photoresist gate. Then the AlGaAs etch would undercut the cap layer and reduce the actual heterojunction to submicron dimensions. The same sort of thing could have been done in the present work with the citric acid etch, but instead the cap layer width was usually left at 4-5 microns and the AlGaAs/GaAs heterojunction

width was usually about 2 microns. This was a simple, high-yield method of producing gates that allowed the critical problems of OM HJFETs to be studied.

The AlGaAs was selectively etched with room temperature HF, as before.[1,2] HF straight from the bottle etched the AlGaAs a little too quickly and so a 1:1 HF:H_2O solution was used. Usually 10-15 seconds was appropriate. The gate etch parameters could be tested with a practice gate etch, performed on a practice wafer included in the OM growth of the gate layers. The practice wafer is then cleaved across the gates and (if desired) stained in HF (to bring out the AlGaAs), then studied with the scanning electron microscope to determine if the gate structure is appropriate.

Some diffusion of Zn from the 1 x $10^{18}/cm^3$ p-AlGaAs to the n-GaAs is to be expected during the OM growth (10 minutes at 730°C). A crude calculation reveals that the p-n junction should be 100-150 Å below the AlGaAs/GaAs heterojunction. Thus after the AlGaAs gate etch there is some chance that a very thin Zn-doped p-layer of GaAs exists on the surface, shorting source, gate, and drain. When a wafer was C-V profiles before and after a gate growth and etch it was determined, with the additional help of point probe tests, that a p-layer did exist. However a 5 sec citric acid etch (nominally 200 Å removed) after the ordinary gate etch made the C-V data quite sensible and showed that not more than 100-200 Å had been removed. Thus the final 5 sec citric acid etch was adopted as part of the gate etch routine.

The p-AlGaAs/n-GaAs heterojunction gate is thick enough (about 0.3 micron) and undercut sufficiently from the p^+-GaAs cap to allow self-alignment of the source, gate, and

drain when a AuGe/Ni/Au metal evaporation, liftoff, and alloy (25 sec at 450°C) is done. This metal forms both the n-type contacts to the source and drain and the p-type contact to the gate. Remarks on contact resistance appear later.

After the AuGe/Ni/Au metallization an electrical test of I-V characteristics can be done on the curve tracer. If the FETs are good enough for further tests the process steps are then completed. First, about 2000 Å of Au is evaporated and lifted off to give appropriate source-gate-drain bonding pads. The wafer is Br-methanol polished from the back to a final thickness of 150 microns and then about 2000 Å of Pd is plated on the back side with an electrodeless technique. The devices are scribed, diced up, and die bonded to gold-plated copper blocks using AuSn preforms. Each source pad (outer pads in Fig. 2) is bonded to ground with 0.7 mil Au wire while the gate and drain are bonded with 0.7 mil Au wires to the 50-ohm input and output lines respectively.

2.3.2 All-OM HJFETs

In the course of this work some difficulty was encountered with the heterojunctions in the VPE/OM HJFETs, owing to the fact that the heterojunction was located at the VPE/OM growth interface. A substantial amount of effort was therefore expended on fabricating HJFETs with n-GaAs active layer as well as p-AlGaAs and p^+-GaAs gate layers grown by OM epitaxy. Table I summarizes the process steps. In order to make a FET with a hetero-junction grown in the OM reactor, it is necessary to grow all three layers at once and thus forego the mesa etch that

TABLE I

ALL-OM HJFET FABRICATION

1) OM growth of n-GaAs/p-AlGaAs/p^+-GaAs on buffer layer.

2) Mesa etch in $NH_4OH:H_2O_2:H_2O$.

3) Gate etch with citric acid and $HF:H_2O$.

4) Deposit 5000 Å CVD SiO_2.

5) Use all-OM mask A to etch squares of oxide on mesa edges at gates.

6) AuGe/Ni/Au or Cr/AuGe/Au metallization and liftoff with all-OM mask B. Alloy.

7) Au overlay, dice and mount, bond in carrier, test.

follows growth of the active layer. When all three layers are mesa etched at once (Fig. 7) the edge of the active layer is exposed. The best mesa etch is 3:1:15 (NH_4OH:H_2O_2:H_2O), which will etch both GaAs and AlGaAs without excessive undercutting of any layer. With the all-OM structure, semiconductor gates can be only on top of the mesa and it is necessary to use the gate metallization to form a gate pad out on the substrate.

After the mesa etch, a gate etch is performed exactly as for the VPE/OM HJFETs. Then about 5500 Å of CVD SiO_2 is deposited and etched with a photoresist mask. There are both electrical and mechanical reasons for a layer of oxide on the edge of the gate (Fig. 7b). The electrical reason is that the edge of the active layer is exposed and would short to the gate metal if the insulating oxide layer was not there. The mechanical reason for the oxide is that a smooth transition from the substrate to the top of the gate is needed or else the metal bridge will open circuit.

The metallization of source, drain, and gate is done with a special mask which is a metal mask for the self-aligned gate HJFET and also provides the needed metal bridge from the gate top to the substrate. Figure 8 shows a completed all-OM HJFET. The metal mask is designed so that the metal avoids the oxide protection areas (four squares at the ends of the gates). The source pads are wider than the mesa to make the probe test easier. The oxide protection squares at the drain pad end of the mesa are nonfunctional in this case but they were included on the oxide mask (four squares appropriately placed) because we might want to extend the gate metal to that end of the mesa by double exposing this mask with an existing gate mask. Following

Fig. 7a Mesa of all-OM HJFET.

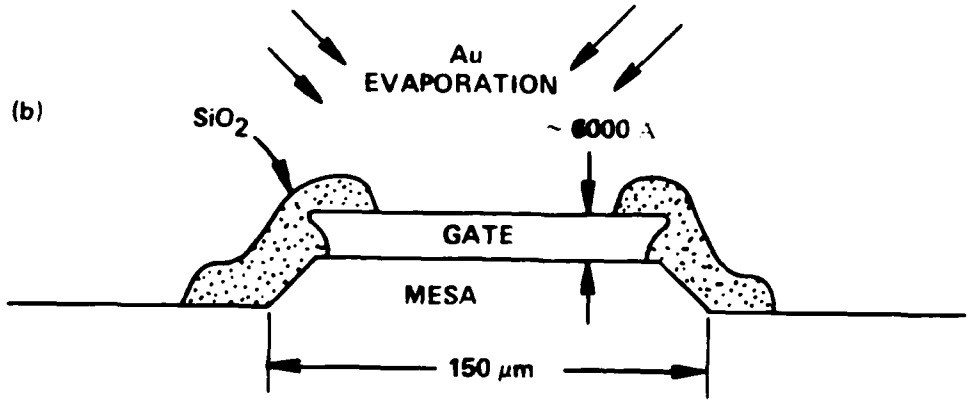


Fig. 7b Side view of gate and oxide protection.
(vertical scale exaggerated)

the metallization step the devices are tested and the rest of the process steps are exactly as with the VPE/OM HJFETs.

By carefully examining Fig. 8, one can see that the gates are broader near the edges of the mesa. This was done by double-exposing the four-square oxide mask with the gate mask using negative photoresist. The gates were broadened in order to minimize source-drain leakage current at the ends of the gates due to undercutting of the AlGaAs.

Before the two special masks for the all-OM HJFET were designed and ordered from an outside supplier, there was an effort to use the existing HJFET mask set to fabricate the all-OM device. This effort, not very successful (discussed in more detail later), involved such things as overexposing and double exposing the existing masks to achieve the desired oxide protection and source-drain-gate metallization. The usual result was unwanted metal shorts from the gate to the source and drain in the vicinity of the mesa edge. Experience gained in this attempt to retrofit our HJFET masks to all-OM helped in the design of the two special masks for the all-OM HJFET.

2.3.3 Al Schottky Barrier FETs

A p-AlGaAs/n-GaAs heterojunction has a built-in voltage of about 1.4 V.[1, 2] A GaAs FET with such a junction as a gate can be simulated by applying a small offset voltage (-0.5 V) to the gate of a GaAs FET with an aluminum Schottky barrier gate. GaAs FETs with 1x200 micron gates fabricated by a self-aligned process[7] were used in an investigation of the channel-substrate interface (Section 2.2) and in the standard test series for heterojunction

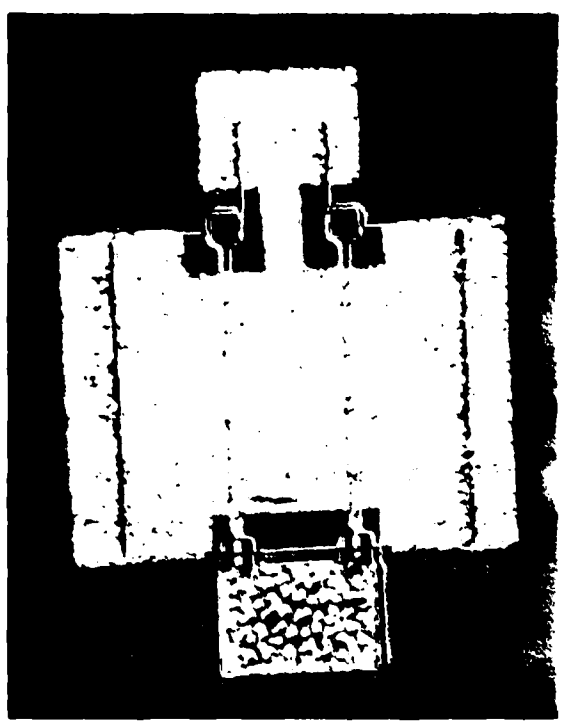


Fig. 8 Top view of completed all-OM HJFET.

FETs. Low frequency I-V characteristics, microwave S-parameters and drain response to fast pulses on the gate were measured in order to evaluate performance possibilities for heterojunction gate FETs. Reference 7 includes details on the fabrication procedure for these Schottky-barrier FETs.

2.4 Experimental Results and Test Procedure

2.4.1 Contact Resistance and Sheet Resistance Measurements

The contact resistance and sheet resistance of each layer of the gate structure were measured using a mask having contact pads with varying source-drain spacings. Organometallic p-AlGaAs/p^+-GaAs was grown on an n-type substrate. The p^+-GaAs was etched away to do the AlGaAs measurements after the contact resistance and p^+-GaAs sheet resistance measurements were completed. Sheet resistance for the GaAs cap layer and the AlGaAs layer were measured to be about 1000 ohms and 2000 ohms per square, respectively. Using measured layer thicknesses and taking mobilities for the p-type GaAs and AlGaAs of 100 cm^2/V-sec, the bulk resistivities were 3.12 x $10^{-3}\Omega$-cm and 6.25 x $10^{-2}\Omega$-cm, giving doping levels of 2 x $10^{19}/cm^3$ and 1 x $10^{18}/cm^3$ for the GaAs and AlGaAs respectively. The specific contact resistance of the metallization was found to be 3.3 x $10^{-4}\Omega$-cm^2 (in agreement with previous work[1]), giving an expected contact resistance for the FET gate of 22Ω. The resistance through the GaAs and AlGaAs adds less than one ohm. The observed gate resistance was always considerably higher than this prediction, as will be seen later.

Contact resistance vs. alloy time was measured for AuGe/Ni/Au on p^+-GaAs, and is plotted in Fig. 9. Recall that AuGe/Ni/Au is used as a contact to both the n-GaAs source and drain and the p^+-GaAs gate in the self-aligned metallization scheme. The contact resistance of AuGe/Ni/Au on n-GaAs is known to be at a minimum when the alloy is done for 25 sec at 450°C,[1] which unfortunately is near the peak of the resistance vs. time curve in Fig. 9. But since the contact resistance of AuGe/Ni/Au on p^+-GaAs varies with time by only a factor of two, this is not of great consequence.

Previous work[1] has also described using AuMg as a gate metallization only while AuGe/Ni/Au is retained as the source/ drain metal. In that work a specific contact resistivity of 5×10^{-6} Ω-cm^2 was found for AuMg on 5×10^{18}/cm^2 p-GaAs. The gates were made by first evaporating and lifting off the AuMg gate metal (2 microns wide), followed by the gate etch. The gate metal was thought to interfere with the undercutting of the semiconductor and problems were encountered with decomposition of Mg in the superoxol gate etch. AuMg metallized gates were etched in this work also. The problem of uneven undercutting of the semiconductor layers was confirmed, very likely being due to the electrical interaction between the metal and the semiconductor. However, replacing the superoxol etch with citric acid eliminated all decomposition problems with the gate etch. It appears that if the AuMg gate metal is deposited and lifted off after the gate etch, there is a good chance that low gate resistance can be achieved, although present lithography techniques allow only wide (7 micron) gates and 2-micron metal stripes. One such experiment was done (on an all-OM HJFET) but while everything seemed in order with the

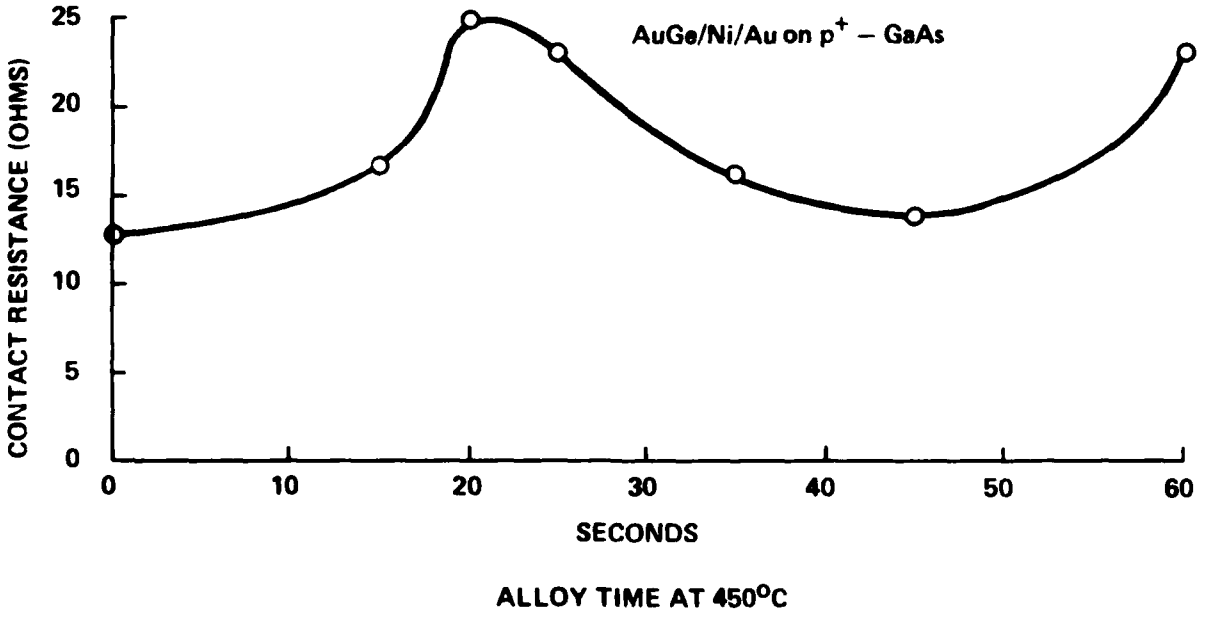


Fig. 9 Interpad contact resistance vs. alloy time for AuGe/Ni/Au on p^+-GaAs.

AuMg metallization, the FETs had other difficulties and the AuMg idea was not satisfactorily tested.

One effort to lower contact resistance to the gate made use of special features of OM epitaxy. The flow of diethyl Zn was maintained at growth temperature, along with an As overpressure, an extra 20 minutes at the end of OM growth of the p^+-GaAs gate layer. The aim was to dope the p^+-GaAs very highly at the surface and thus lower contact resistance to the metal. A few FETs were made in this way, but it could not be conclusively shown that gate resistance was lower. Contact resistance measurements using methods described above were also inconclusive because of temporary difficulties with the metallization and alloy. There was some evidence to suggest that the interpad resistance was very low, which is to be expected if heavy surface doping was achieved. But because of AuGe/Ni/Au bubbling, the probe resistance through the metal varied a lot and was comparable to the interpad resistance, so hard numbers for contact resistivity could not be obtained.

2.4.2 Ion-Implanted Active Layers

HJFET active layers made by ion implantation of Si^{28+} through Si_3N_4 into a VPE buffer layer were briefly investigated with the ultimate aim of comparing carrier velocity profiles to those of buffered and unbuffered VPE active layers. An implant of $3.2 \times 10^{12}/cm^2$ at 180 keV was done into a wafer held at 221°C. However, HF etch rates and ellipsometric measurements of refractive index revealed that the Si_3N_4 films, deposited at LFE Corp., contained too much oxygen for a satisfactory anneal. Then a 1000 Å film of Si_3N_4, free of oxygen, was deposited at 300°C at the

University of Illinois. After the implant the wafer was annealed at 800°C for 30 min in forming gas. The layer was intended to be $10^{17}/cm^3$ doping and 4V pinchoff but instead was $3 \times 10^{17}/cm^3$ and 13V pinchoff, the reason being that calibration of the implantation parameters had been done earlier with the oxygen-rich Si_3N_4. When oxygen is present in Si_3N_4, the implanted species tend to diffuse into the encapsulant and thus lower the activation percentage.

2.4.3 Al Gate Schottky-Barrier FETs

As mentioned in Section 2.3.3, Al gate Schottky-barrier FETs were made to simulate the heterojunction gate FET. The experiments with buffered normally-on SBFETs to evaluate the channel-substrate interface have already been discussed in Section 2.2.

Complete high frequency measurements were made on wafers from two SBFETs, TRS 18-2 and TRS 24-10. I-V curves appear in Fig. 10. TRS 18-2 was normally-off with only the Schottky barrier, i.e., V_p = OV. TRS 24-10 had V_p = -0.7V. Microwave S-parameters were measured, then converted to Y-parameters and fit to a circuit model. Figure 11 shows the high frequency circuit models for these FETs. R_s was determined by a dc measurement. Table II summarizes some dc and microwave performance parameters for these buffered SBFETs.

Large-signal switching measurements of the kind made previously[1,2] were carried out for the SBFETs in order to determine intrinsic propagation delays. Some changes were made in the design of the microstrip bias circuit in order to couple more of the output pulse into the sampling scope than before. The scheme used for the measurement is shown

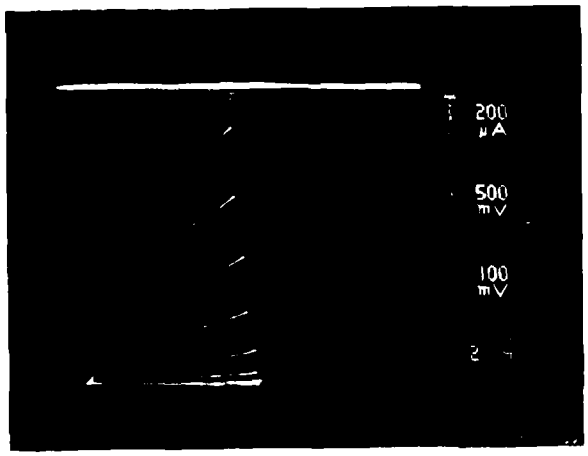
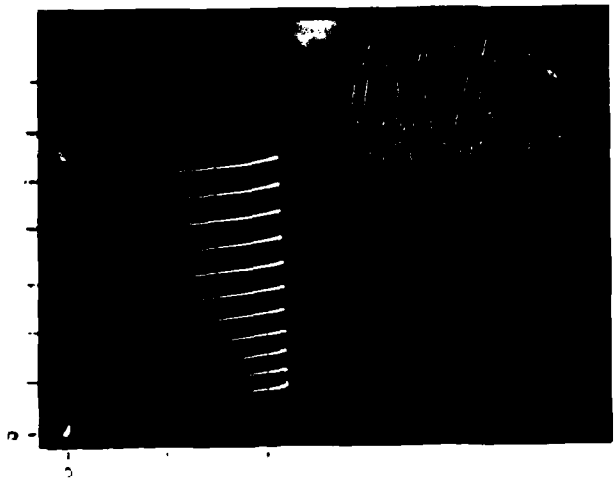
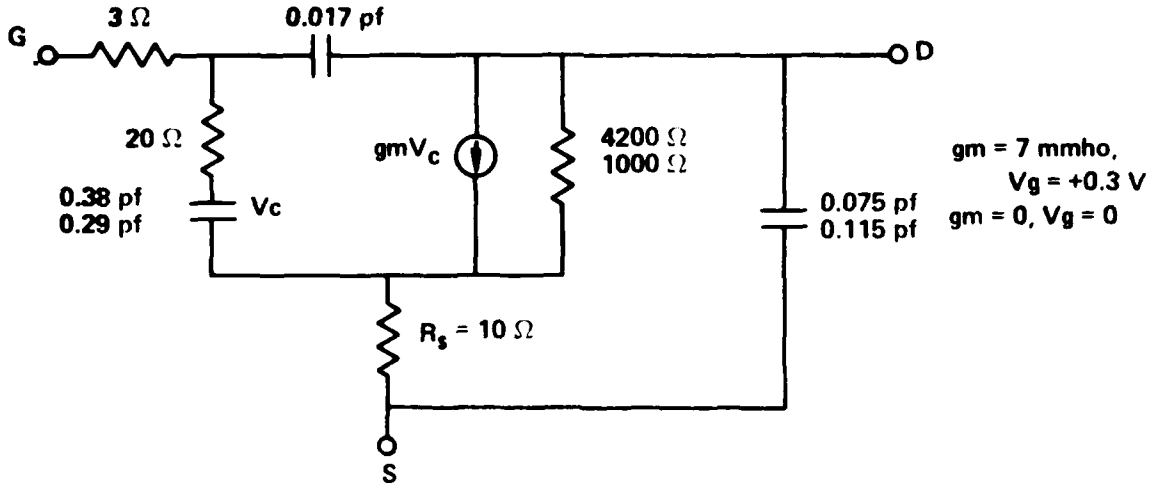


Fig. 10a I-V characteristic for TRS-18-2

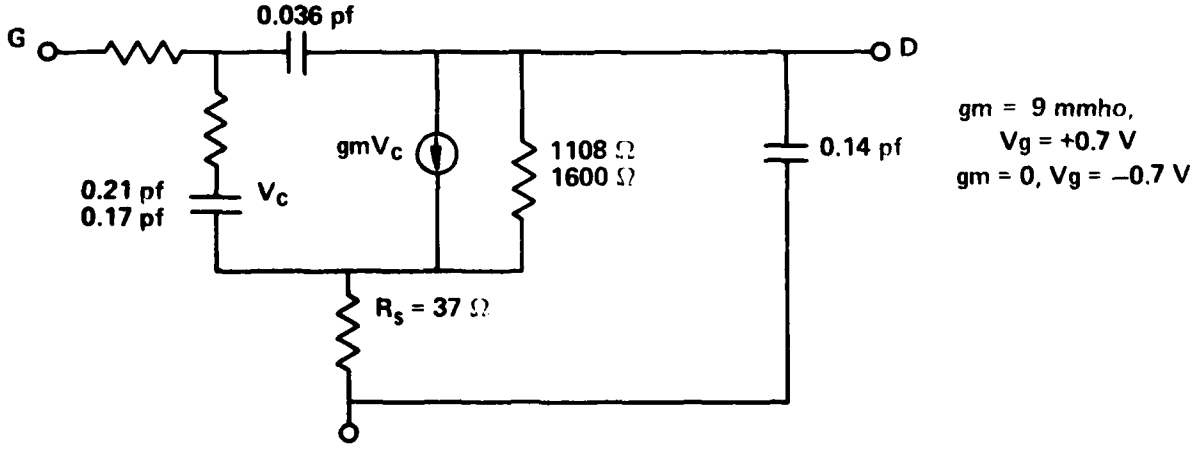


2 mA/div
1 V/div
100 mV/step
-.5 V gate offset

Fig. 10b I-V characteristic for TRS 24-10.



TRS 18-2 NORMALLY-OFF SBFET (Vp = 0V), Vg = +0.3 V
(LOWER VALUES ARE FET OFF, Vg = 0 V)



TRS 24-10 #1 SBFET (Vp = –0.7 V), Vg = +0.7 V
(LOWER VALUES FOR FET OFF, Vg = –0.7 V)

Fig. 11 Circuit models for Schottky-barrier FETs.

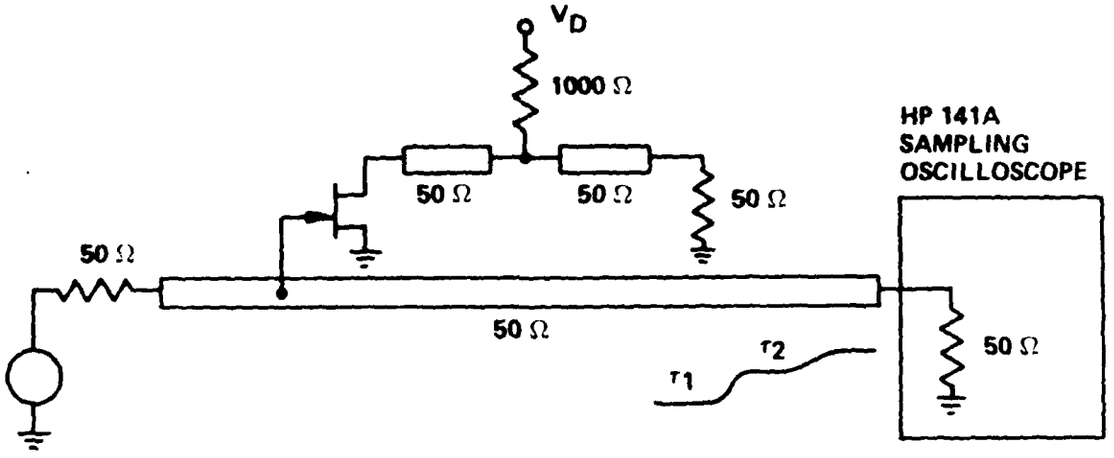
TABLE II

SUMMARY OF SBFET RUNS

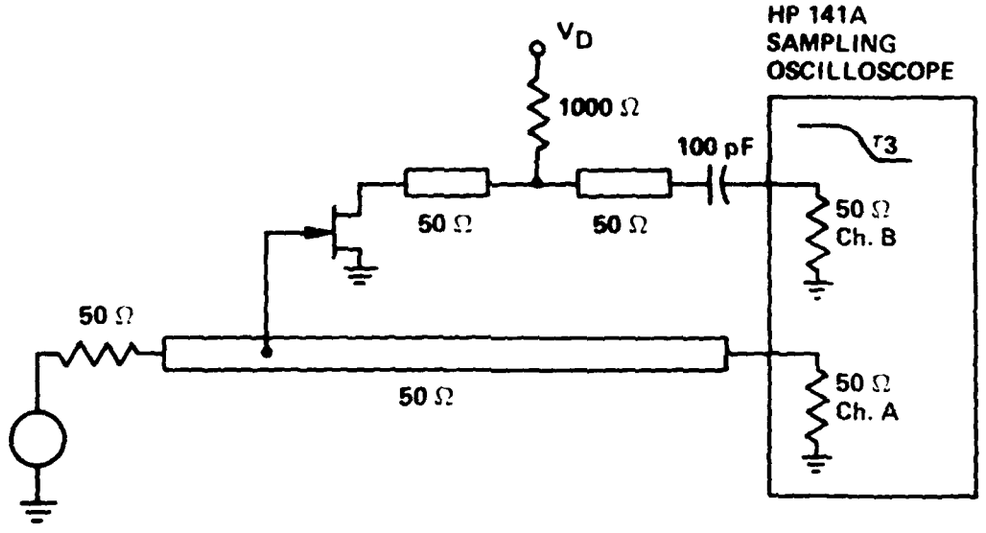
Wafer No.	V_{po} (V)	g_m (mmhos)			Microwave g_m at V_g=+0.5V (mmhos)
		V_g=+0.5V	V_g=0 V	V_g=-0.5V	
TRS 18-2	0.0	5	0	-	-
TRS 22-2	-0.5	3	1.6	-	2
TRS 24-10 typ	-0.5	12	10.0	8	9
TRS 24-10 high	-0.8	27	20.0	10	-

in Fig. 12. The bias network connects to V_D, the sampling scope, and the drain of the FET. Blocks labeled 50Ω refer to 50Ω transmission lines. Reference 4 contains other details of the pulse measurement apparatus, including pictures.

First, a pulse having a rise time of about 5 nsec is sharpened to about 200 psec with a step-recovery diode (HP 5082-0008) and fed into the test circuit. The gate capacitance charging time is then measured by using the reflection of the input gate pulse. Figure 12a shows the measurement setup and Fig. 13a a typical sampling scope trace. Then the apparatus is assembled as in Fig. 12b and the transmission line length through the FET bias network is equalized with the input signal transmission line length on the other sampling scope channel. The fall time of the drain voltage can then be measured (Fig. 13b) and compared with a zero-delay response deduced from the low-frequency I-V curves. Often in these measurements the FET was operating in a linear bias region so that the propagation delay could be estimated from the sampling scope traces. The method used is illustrated in Fig. 14, on which are schematically drawn the oscilloscope traces from Fig. 13. Results for normally-off SBFETs TRS 18-2 #3 and TRS 18-2 #2 and normally-on SBFET TRS 24-10 #1 are in Table III. The "estimate" column contains results from the Fig. 14 method. Figure 15 illustrates how the propagation delay was derived for TRS 24-10 #1. The 27-psec delay for TRS 24-10 #1, with V_p = -0.7V and therefore nearly a simulated normally-off HJFET, is a considerable improvement over the 69 psec of the normally-off SBFET (V_p = 0V), TRS 18-2 #3.

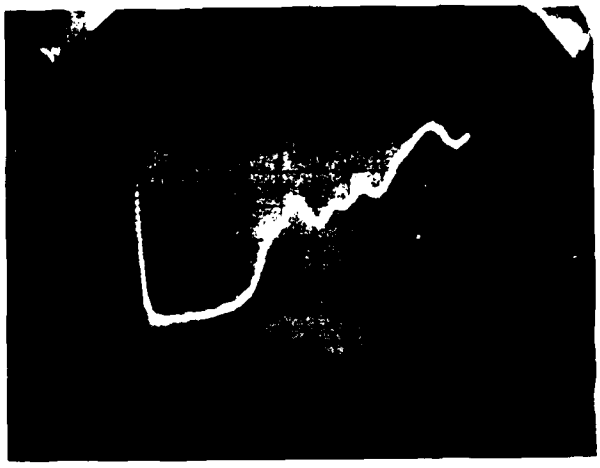


(a) INPUT CAPACITANCE CHARGING TIME DETERMINATION



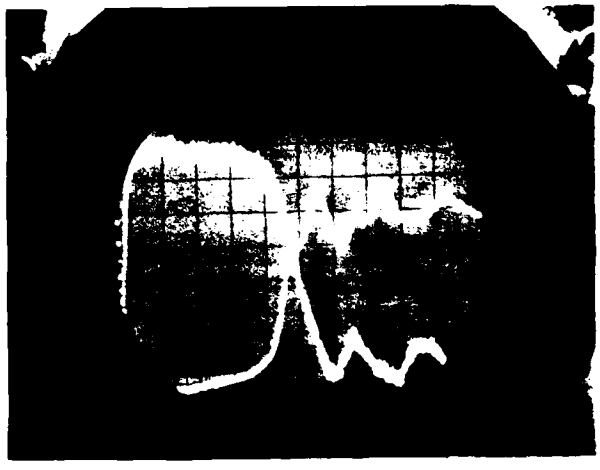
(b) PROPAGATION DELAY TIME DETERMINATION

Fig. 12 Switching speed measurement scheme.



200 psec/div
20mV/div

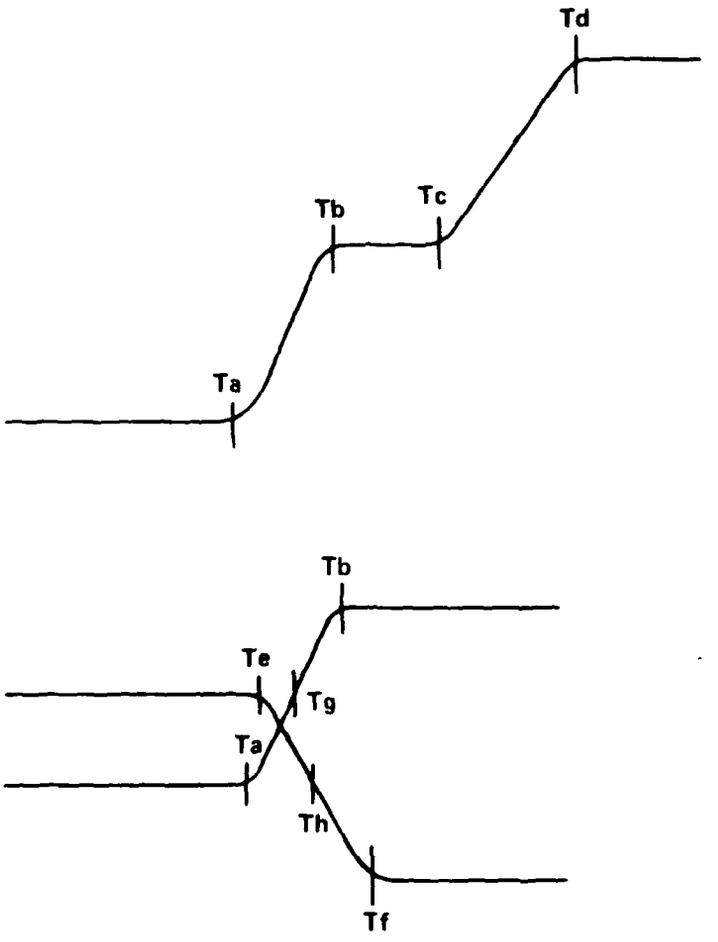
Incident Gate
Pulse and
Reflection



200 psec/div
10mV/div drain
20mV/div gate

Incident Gate
Pulse and
Drain Response

Fig. 13 Switching Characteristics of Normally-Off Schottky Barrier FET (TRS 18-2#3)



$T_1 = T_b - T_a$	INPUT GATE PULSE RISE TIME
$T_2 = T_d - T_c$	REFLECTED GATE PULSE RISE TIME
$T_f - T_e$	DRAIN RESPONSE FALL TIME
$T_3 = T_2 - T_1$	GATE CAPACITANCE CHARGING TIME
$T_e - T_a$	RESPONSE TIME
$(T_h - T_g) - T_3$	ESTIMATED PROPAGATION DELAY

Fig. 14 Measurement of switching and delay times.

TABLE III

SWITCHING AND DELAY TIMES FOR SBFETs

(all times in picoseconds)

Device #	g_m	T_1 Gate Rise	$T_2 - T_1$ Gate Cap. Charging Time	$T_e - T_a$ Response Time	$T_f - T_e$ Drain Fall Time	$(T_h - T_g) - T_3$ Propagation Delay Estimate	Actual
TRS 18-2#3	10	349	10	36	365	53	68.5
TRS 18-2#2	5	321	10	90	344	118	109.0
TRS 24-10#1	25	334	10	40	370	30	27.0

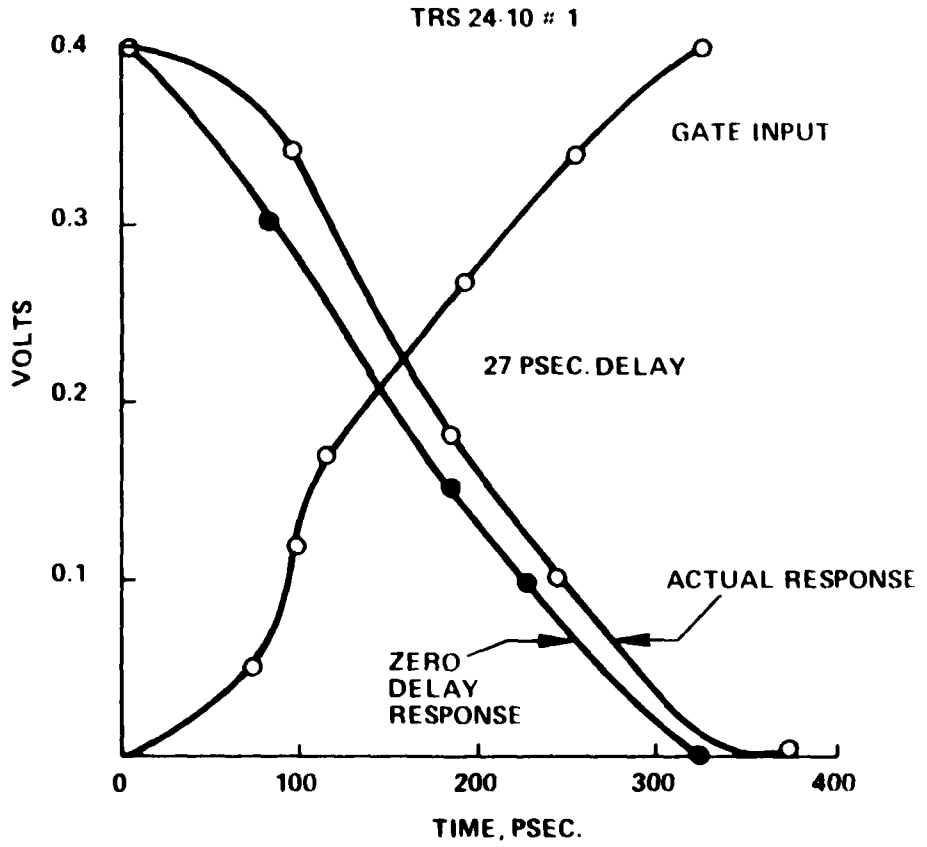


Fig. 15 27 PSEC. PROPAGATION DELAY TIME THROUGH NORMALLY ON SCHOTTKY BARRIER FET

2.4.4 Ring Oscillators and Inverters

One of the reasons for developing a good heterojunction gate FET is to use the same technology in a small-scale integrated circuit that would demonstrate the viability of normally-off HJFET logic. Such a circuit is the ring oscillator (RO), a string of inverters an odd number of stages long, which loops back on itself and whose oscillation frequency is determined by the number of stages and the time required for one inverter to switch the next. A mask set for 11- and 21-stage ROs was already in existence and was used to process a few wafers in order to see how the HJFET technology transfers. Figure 16 shows the basic inverter circuit and the layout of the components on the chip for one RO stage. For one set of ROs, inverter gates are 3x100 microns and active load gates are 3x33 microns. A smaller set has gates about two-thirds that size. Photographs are in Fig. 17. As can be seen in Fig. 17b, the mask also contains basic inverter stages with pads at every connection.

Fabrication of the ROs and inverters proceeds exactly as does HJFET fabrication (Fig. 5) with the exception that after step 6 (which in this case is not a self-aligned metallization), wherein AuGe/Ni/Au was alloyed, the metal mask is used again to lift off 5000-6000 Å of Al so that there will be a metal bridge where the gates connect to the rest of the circuit (Figs 16 and 17a).

The first ROs were fabricated early in the program, using some of the very first OM gate layers. The inverter

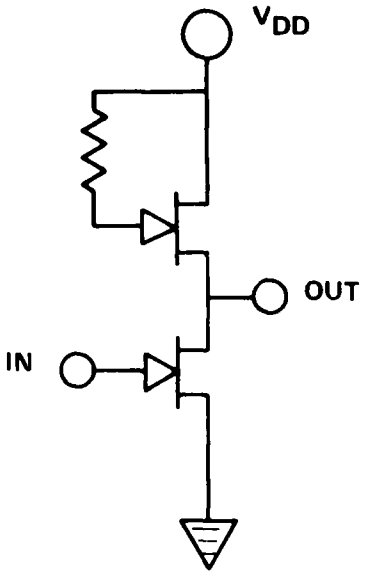


Fig. 16a Basic inverter circuit.

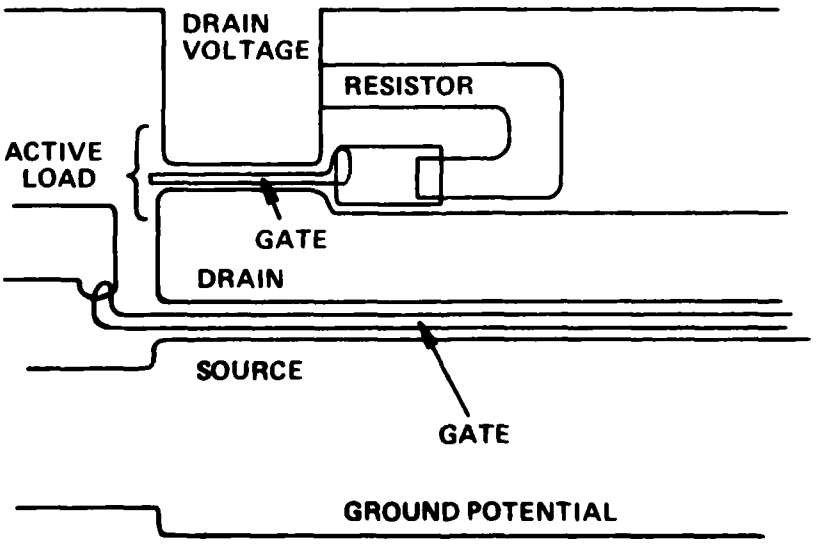


Fig. 16b Layout of inverter in ring oscillator.

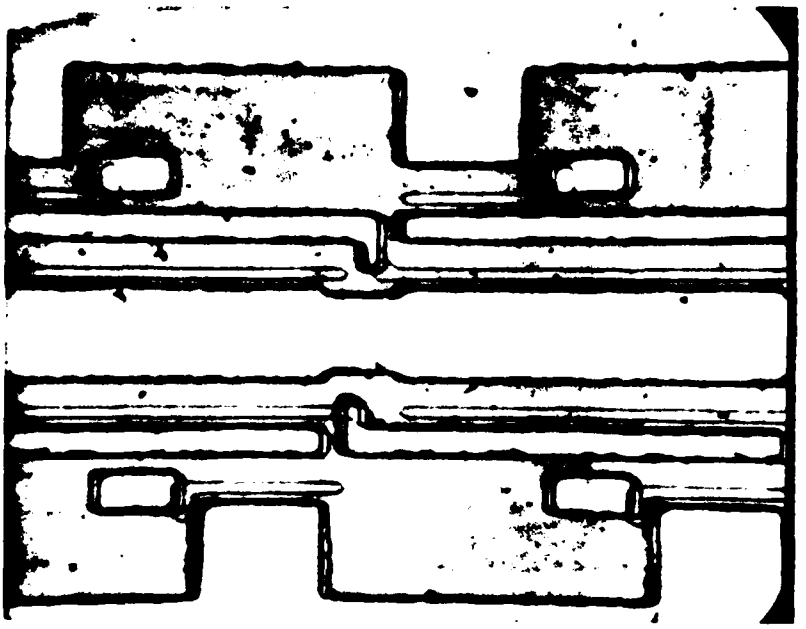


Fig. 17a Detail of ring oscillator.

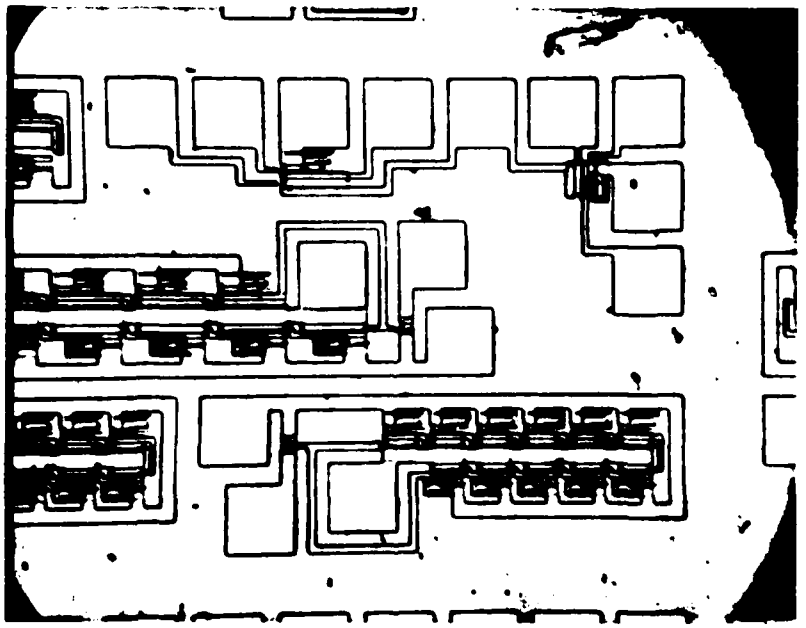


Fig. 17b Inverters and ring oscillators.

transistors and active loads were highly resistive because it was not known that the HCl flow in the OM reactor was etching off the active layer before gate growth. This was easily corrected by delaying the HCl flow, but other difficulties with the basic FET forced attention away from ROs and back to HJFETs alone.

Later on in the program, when all-OM technology (Sec. 2.3.2) had been substantially worked out, one wafer of all-OM ROs was processed using the same kind of retrofit mask techniques that were used with the HJFETs. The retrofit oxide protection (a stumbling block for the HJFETs) worked here because the RO FETs are not self-aligned. However, there was difficulty making metal bridges to the gate on top of the mesa because of gate overhang and 3-layer mesa-etch undercut. These problems were emphasized by the small mesas in the RO circuits and helped lead to improvements in the all-OM process (e.g., one-step mesa etch). The all-OM RO may be developed further when all-OM HJFETs (results below) are perfected.

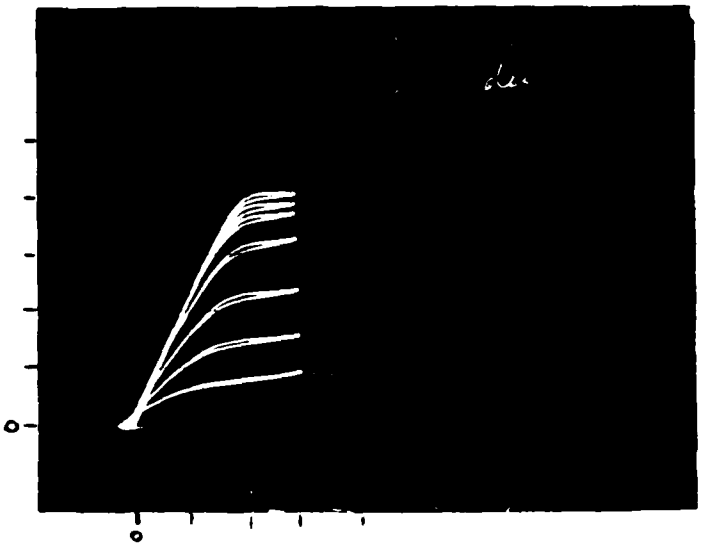
2.4.5 All-OM HJFETs

The first attempts to fabricate an all-OM HJFET (Section 2.3.2) involved a retrofit of the mask set used for the VPE/OM HJFET. Oxide protection on the edge of the mesa had to be done by using negative photoresist and overexposing the self-aligned mask at a slight distance from the wafer. Then the oxide was etched in buffered HF. The problem was that the self-aligned metal mask (which was double-exposed with a gate mask to connect the gate pad)

would deposit metal near the gate ends and the oxide layer would cause source-gate-drain shorts. Efforts to use gate masks to etch away the offending parts of the oxide la er failed because other shorts would usually develop. One rather rare example of an all-OM HJFET that showed FET-like I-V curves is pictured in Fig. 18. While the gate does not rectify satisfactorily (Fig. 18b), the device otherwise behaves like a normally-on HJFET (Fig. 18a). Notice the crowding of curves near I_{DSS} for small gate voltages. Some kind of problem seems to exist at the heterojunction interface (a heterojunction grown in the OM reactor), although conclusions cannot be drawn from such an irreproducible FET as this. We will return to this point in discussions that follow.

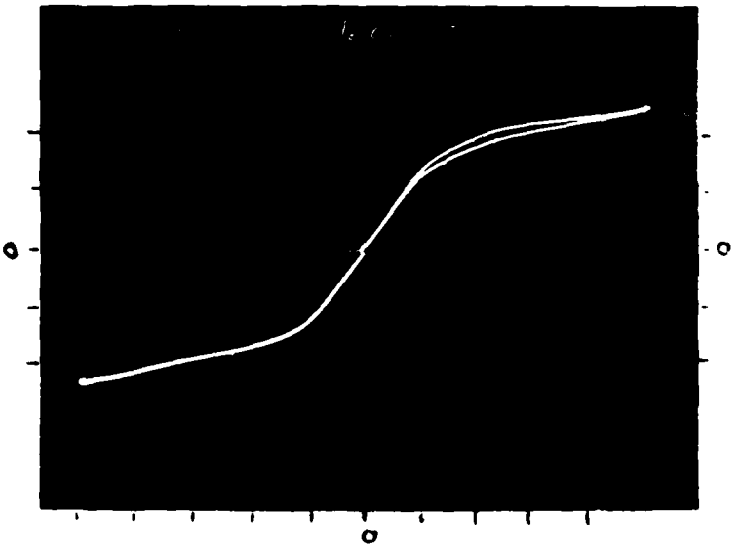
Once the special all-OM HJFET masks were acquired and used along with the other HJFET masks to make all-OM HJFETs, some more satisfactory devices were made. I-V curves for one are in Fig. 19. This time the gate I-V curve (Fig. 17b) is much more satisfactory, although the 2K forward resistance is much like that of VPE/OM HJFETs. The crowding of curves near I_{DSS} in Fig. 19a points to another interfacial problem, possibly traps (suggested also by the loops). Again this is a heterojunction grown in the reactor, and so the kind of interfacial problem one might expect at a growth-interface heterojunction (as with VPE/OM) can be ruled out.

The transistors of Fig. 19 were from a wafer with fairly low yield because the metallization was straight AuGe/Ni/Au. Many gate pads were disconnected from gates on account of gate metal breaking as it crossed the oxide (Fig. 20a). Later on the Cr/AuGe/Au metallization (Section 2.3.2)



V: 10 ma/div
H: 1 V/div
-1 V/step

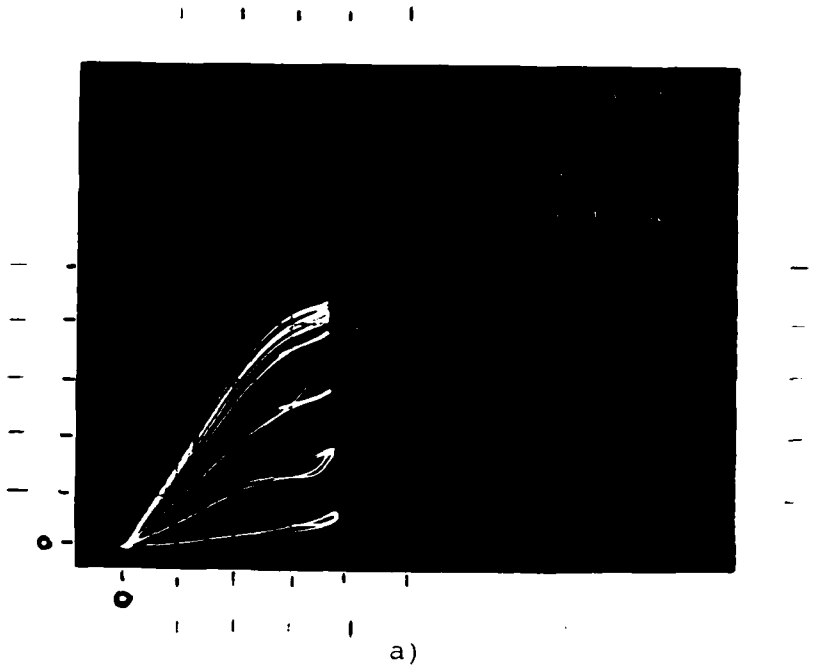
(a)



V: 1 ma/div
H: 1 V/div

(b)

Fig. 18 First all-OM HJFET (retrofit, OM 403).
a) I-V characteristic of (normally-on) all-OM HJFET.
b) Gate-to-source characteristic of all-OM HJFET.



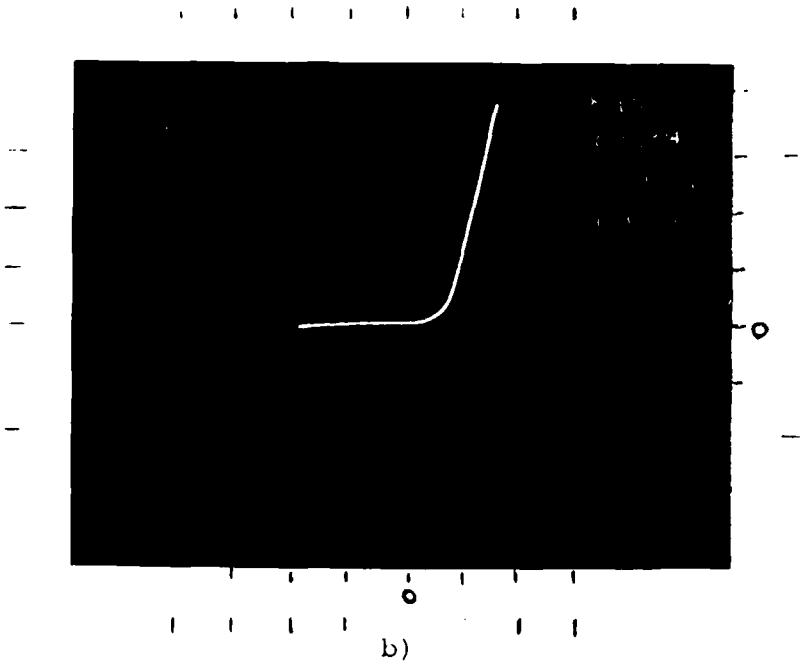
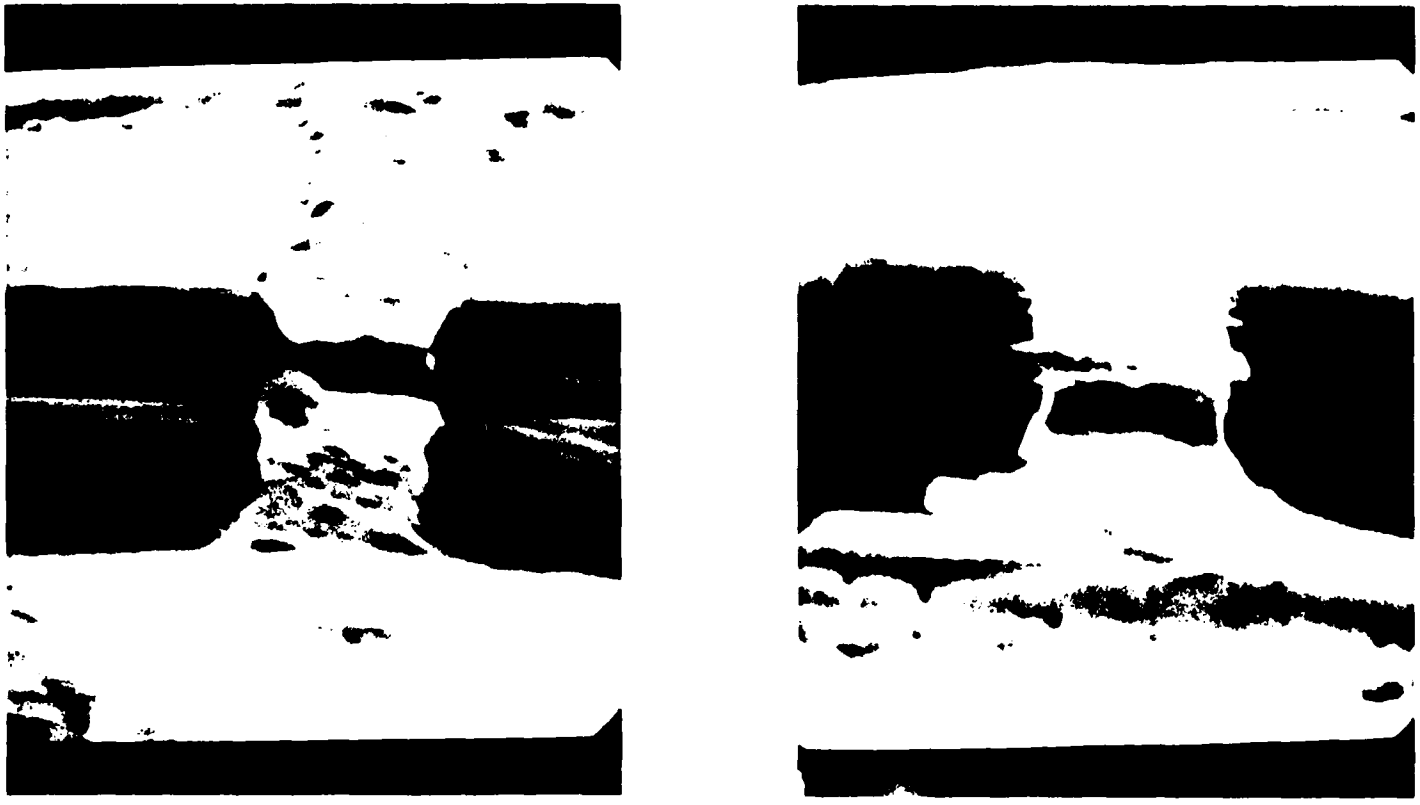


Fig. 19 All-OM HJFET produced with new masks (OM 505).

a) I-V characteristic of (normally-on) all-OM HJFET.

b) Gate-to-source characteristic of all-OM HJFET.



(a) (b)

Fig. 20 Gate metal over oxide in all-OM HJFET.
Connecting stripe is 2 μ wide.
a) AuGe/Ni/Au metal break.
b) Metal bridge with Cr/AuGe/3-step Au.

was found to work much better (Fig. 20b) although some of its success was probably due to the Au evaporation being in three steps, two at a slant (Fig. 7b). As this work was done late in the program, there was no opportunity for the obvious tasks of measuring the Cr/AuGe/Au contact resistance and of trying 3-step Au on AuGe/Ni/Au.

The best yields of all-OM HJFETs were obtained when the gates were aligned parallel to 3:1:15 ($NH_4OH:H_2O_2:H_2O$) etch pits, i.e., in the (011) direction. Gates aligned perpendicular to this direction seemed to develop metal breaks between gate pad and gate more often, although a more thorough study using a Cr/AuGe/Au metallization is needed.

Some problems were encountered due to difficulties in reproducing the desired OM gate layers with every run. On the all-OM HJFETs with the successful Cr/AuGe/Au metallization, for example, the gates were shorted to source and drain because the AlGaAs layer was only about 1000 Å thick, even though when the growth parameters were set some months earlier the layer was more than twice that thickness.

During OM growth of the transistor layers an n^+-GaAs substrate was always included in the reactor as a practice wafer. This would be used for practice gate etches (Section 2.3.1) and often for 20-mil heterojunction diodes made by evaporating and alloying 20-mil AuGe/Ni/Au dots, then mesa etching the p-layers. The best back contact could be made by evaporating AuGe/Ni/Au on a polished backside of the substrate before the whole wafer was alloyed.

Figure 21 shows a typical I-V curve for a HJ diode made from an all-OM (n-GaAs/p-AlGaAs/p^+-GaAs) growth on an n^+ substrate. Notice that the voltage scales for forward and reverse bias are different. The diode's forward resistance is about 40 ohms, a typical value for these heterojunctions. As a control, a 20-mil Schottky dot on n/n^+ GaAs was measured and found to have 8 ohms forward resistance. Forward resistance of HJ diodes ranged from 10 ohms to several hundred ohms and was a rough indicator of heterojunction quality. But generally the HJ diodes were not a very informative diagnostic test except when they showed excessive reverse leakage and spared us the trouble of making HJFETs.

2.4.6 VPE/OM HJFETs

Most of the work in this program centered around the VPE/OM HJFET, processed as described in Section 2.3.1. The fabrication technology of a perfected VPE/OM HJFET could be readily transferred to the ring oscillator for a test of normally-off heterojunction logic. The VPE/OM HJFET has a heterojunction grown at the VPE/OM growth interface and so careful preparation of the surface before OM growth is necessary.

A few initial OM runs were needed to set growth parameters for proper layer thickness and solve the HCl problem discussed above. Then once a satisfactory gate etch procedure was established, the first FETs were made. These first FETs suffered from extremely leaky gates and a variety of other symptoms, including poor surface morphology after OM growth. Improvements in the wafer preparation

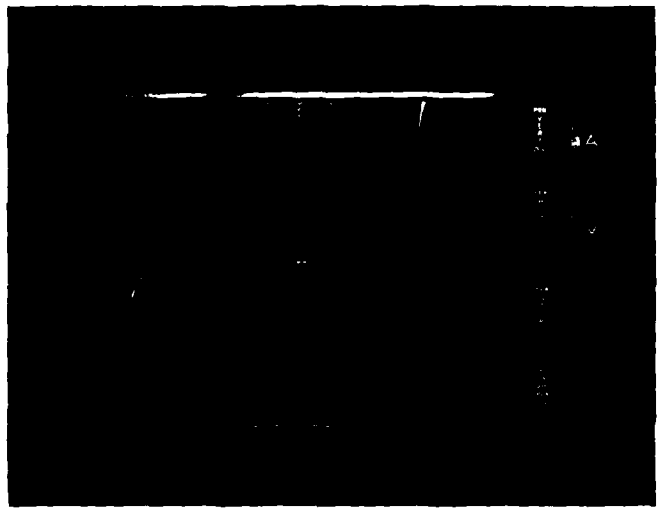
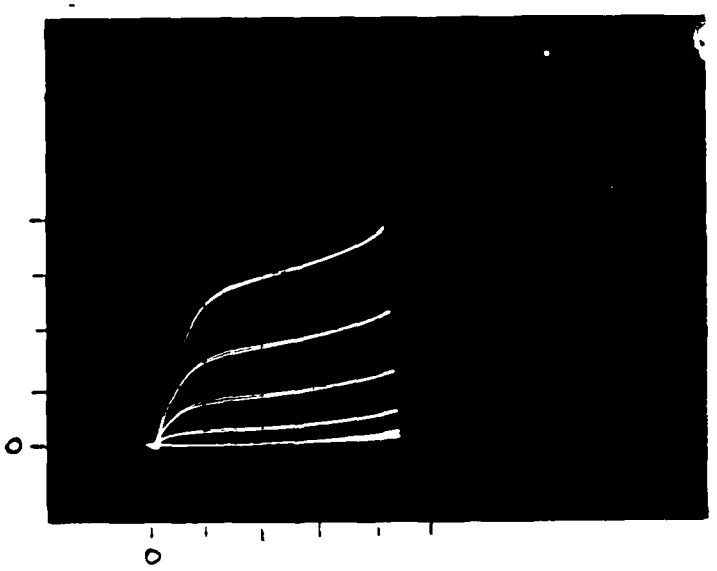


Fig. 21 20-mil heterojunction diode (OM-509).
Forward: 1 ma/div, 200 mV/div.
Reverse: 10 μA/div, 1 V/div.

before OM growth were apparently needed. An aurostrip dip prior to OM growth, even if followed by a prolonged rinse, did not usually produce a good surface after OM growth. The best procedure was to follow the mesa etch by cleaning in A40 photoresist strip and rinsing in isopropyl alcohol. Often there would be evidence of gold C-V dots on the wafer both before and after OM growth. When gold dots were not left on the wafer for a long time (more than a few days) this would not happen.

Even with good surfaces after OM growth, the heterojunctions were quite often leaky. Since the heterojunction was at the VPE/OM growth interface, and since no meltback occurred as with LPE, it was felt that the wafer preparation immediately before OM growth must be crucial. Several experiments were done with 4:1:1 and 10:1:1 (H_2SO_4:H_2O_2:H_2O) wafer dips (several seconds), which etch the layer slightly. The 10:1:1 seemed to work as well as 4:1:1 and is preferred because it etches the layer less. Experiments with pure H_2SO_4, which does not etch the GaAs at all, produced less satisfactory results. However, no wafer preparation consistently solved all interfacial problems. Once the all-OM HJFET experiments suggested that the interfacial problem was linked to the OM material itself, the wafer preparation results were better understood.

The best normally-off HJFETs come from TRS 30-4B and two typical I-V curves are shown in Fig. 22. The threshold voltage of +1V indicates an interfacial problem. Several other wafers also produced normally-off HJFETs, but with threshold voltages of 2-4V.



V: 5 ma/div
H: 1 V/div
+1 V/step

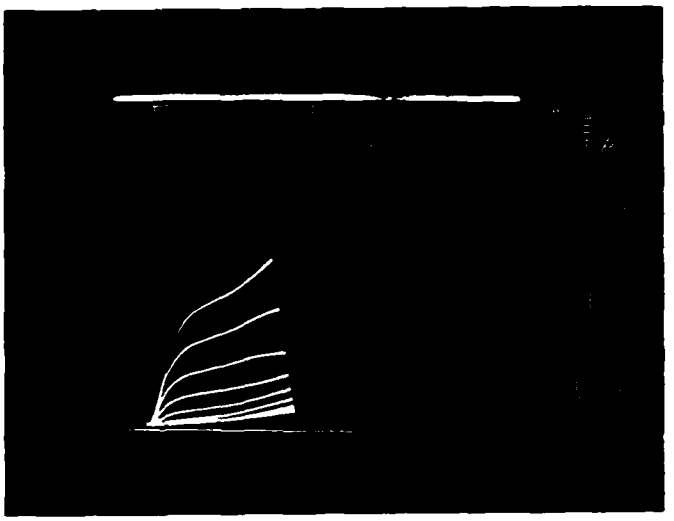


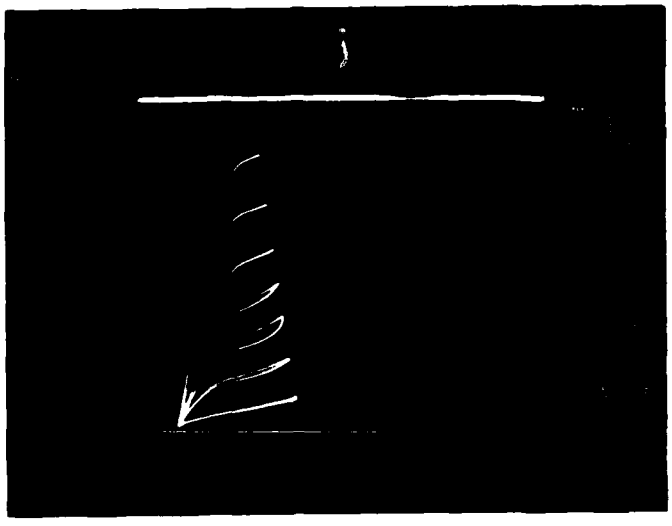
Fig. 22 Two typical I-V curves of normally-off VPE/OM HJFETs.
(TRS 30-4B)

A good many normally-on VPE/OM HJFETs were made because it was always safest to start with a thick epitaxial layer when one did not know how much material the wafer prep would etch off. Many of these had the apparent interfacial trap problem, with crowding of I-V curves near I_{DSS}. However, wafer B24-10 (OM 450), prepared with a 4:1:1 etch and a slight HCl *in situ* etch just before OM growth, yielded some good normally-on HJFETs with V_p = 6-8V and g_m up to 12 mmho. I-V curves appear in Fig. 23. The usual crowding of curves near V_g = 0 was somehow avoided and so the OM 450 HJFETs were deemed worthy of high frequency and switching measurements.

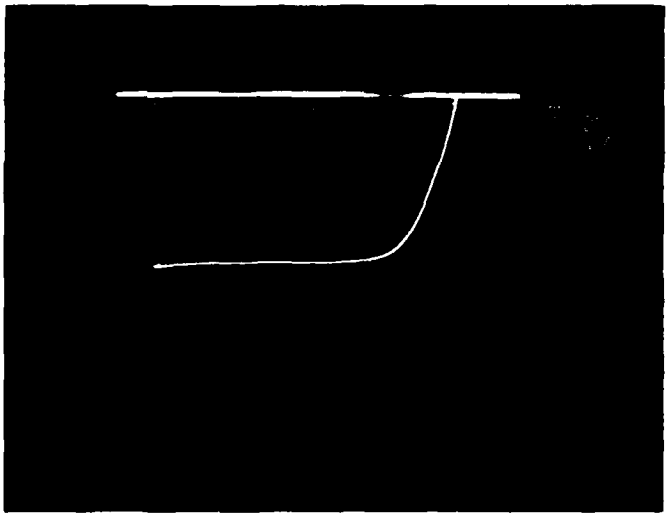
Microwave S-parameters were measured, converted to Y-parameters, and fit to a circuit model as described in Section 2.4.3. Figure 24 shows the model and the component values as a function of gate bias. Equivalent circuit values for this FET can be compared to those for the N-on HJFETs made by LPE[1, 2] which were measured at 3.3V drain voltage. The present FETs have lower g_m and higher R_d and R_g than the earlier LPE HJFETs.

Large signal pulse measurements, also as described in Section 2.4.3, were made on the same FET. Sampling scope traces, as in Fig. 25, were analyzed as in Fig. 14 to reveal a gate capacitance charging time of 10 psec and a propagation delay of 47 psec. The propagation delay was almost invariant from V_g = +1V to -4V. By comparison, earlier [illegible] LPE HJFETs[1,2] had propagation delays of 20 psec.

The general inferiority of these VPE/OM HJFETs to earlier LPE HJFETs is not surprising since so few of the present series worked well enough to be given a complete



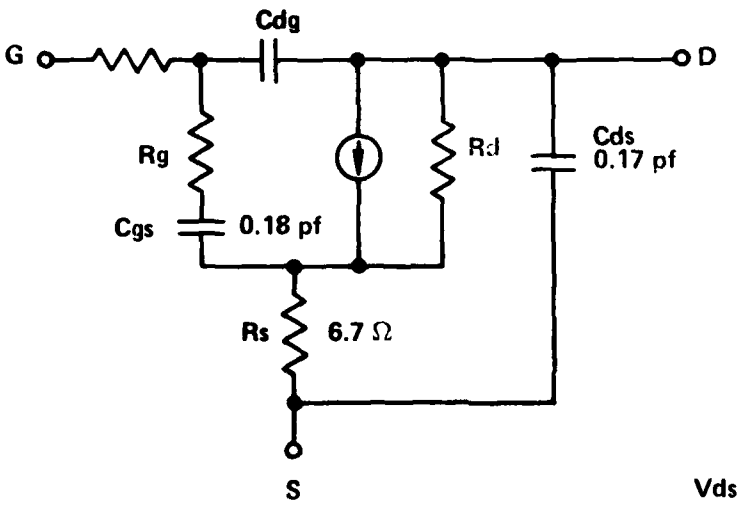
a) FET I-V characteristic.



b) Gate-to-source characteristic.

Fig. 23 Normally-on VPE/OM HJFET (OM 450).

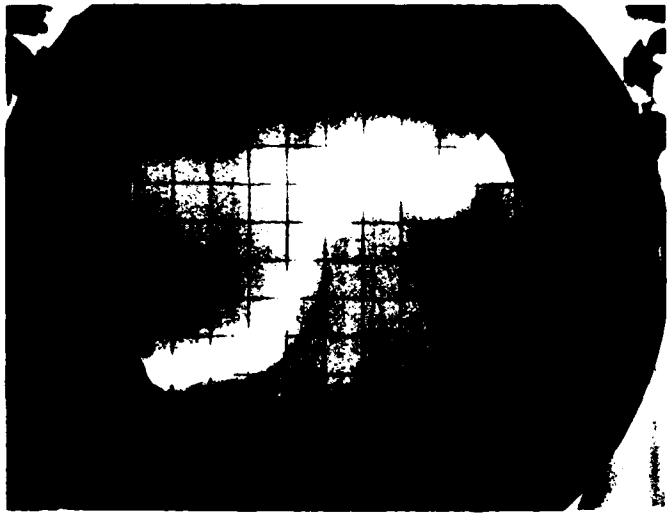
CIRCUIT MODEL OF HJFET – OM450



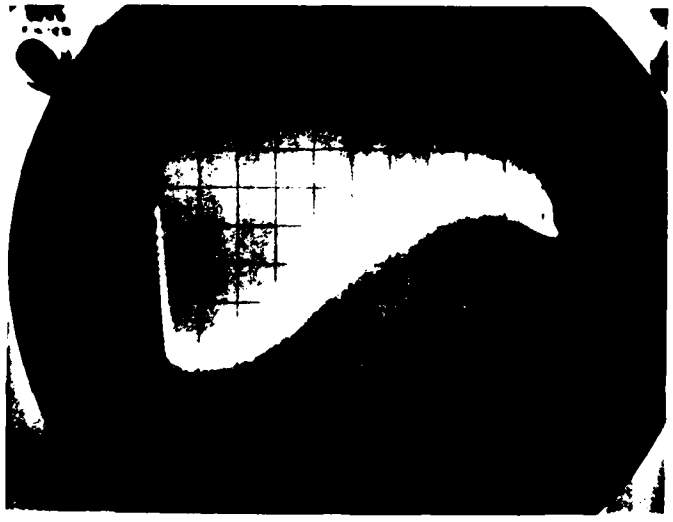
Vds = 4 VOLTS

GATE BIAS	Rg	Cdg	Rd	MAX GAIN AT 3 GHz	gm at 2 GHz
+1.0 VOLT	–	0.01 pf	800 Ω	9.4 dB	2.7 mmho
0	48 Ω	0.02	800	7.8	5.9
–2.0	46	0.022	800	7.1	5.7
–4.0	40	0.028	1400	4.5	2.7

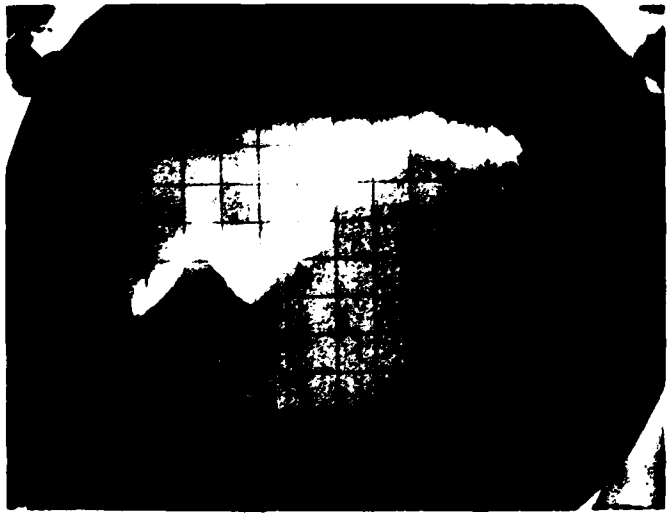
Fig. 24 Circuit model and 3 GHz gain of OM 450 N-On VPE/OM HJFET.



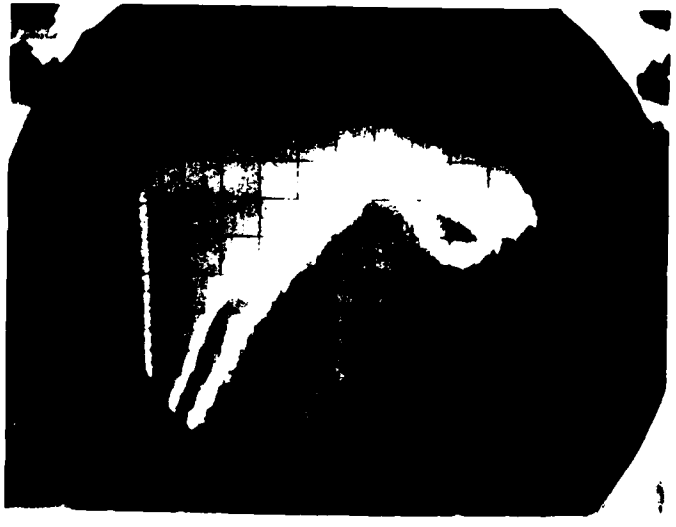
a) Incident gate pulse, 100 psec/div.



c) Incident gate pulse and drain response (inverted and scaled), 50 psec/div.



b) Reflected gate pulse, 100 psec/div.



d) Incident gate pulse and drain response (vertical scale magnified), 50 psec/div.

Fig. 25 OM 450 N-on VPE/OM HJFET pulse measurement.
Prepulse bias conditions were V_{ds} = 4V, V_g = -2V.

series of tests. Moreover, the gate lengths here were 2-3 microns while the earlier HJFETs had submicron gate lengths. Also the majority of these VPE/OM HJFETs suffered from severe problems with the OM material, and it is likely that some of those same problems existed with OM 450 which was chosen for tests.

2.5 Discussion

The HJFET results presented in the preceding sections strongly indicated a trap problem at the AlGaAs/GaAs heterojunction interface. VPE/OM normally-off FETs had threshold voltages of from +1 to +4V, and every all-OM HJFET (normally-on) showed crowding of the I-V curves near $V_g = 0$ (Figs. 18 and 19). Normally-on VPE/OM HJFETs showed evidence of interfacial traps in the same way as the normally-on all-OM HJFETs.

As stated before, the interfacial problem with VPE/OM HJFETs could have been due to the difficulties of growing a heterojunction at the VPE/OM interface. Indeed, this was thought to be the case until the all-OM HJFETs could be made, near the end of the program. The all-OM HJFETs showed that an interfacial problem existed even when the heterojunction was grown in the OM reactor. Moreover, at the same time that the all-OM HJFET result was acquired, there was a similar AlGaAs/GaAs interfacial trap problem with solar cells grown in the same reactor. Finally some analysis of OM AlGaAs layers made by secondary ion mass spectrometry (SIMS) showed that a substantial amount of oxygen is in the AlGaAs. Since oxygen produces the kind of bulk and inter-

facial contamination in AlGaAs that would cause electrical behavior of the kind observed with the HJFETs, the source of our difficulties appears to be identified. Oxygen-free AlGaAs will have to be grown before good HJFETs can be made.

3. RECOMMENDATIONS FOR FURTHER STUDY

In the previous section we concluded that oxygen-free gate layers must be grown before a good HJFET can be made. Once this is accomplished (with organometallic or molecular beam epitaxy (MBE)), the doping concentration in the AlGaAs layer should be verified to be at least $1 \times 10^{18}/cm^3$ so that almost all of the reverse voltage is dropped across the channel depletion layer. Then the HJFETs can be tried once again.

If normally-off VPE/OM HJFETs could be made, the processing would be simplest and could be readily transferred to the ring oscillator, as described earlier. The wafer preparation before OM growth may be critical, as before. One possibility with improved OM material would be to rinse the wafer in H_2SO_4 before OM growth, which may clean and dehydrate the surface adequately. Another would be to dip in HF, blow off, then rinse in H_2SO_4 before loading. The first step would remove any oxides and the second would remove moisture, including any picked up from the HF dip. The same general procedures might be used with MBE. Such wafer preparation without etching of the active layer is preferred because one can easily prepare active layers with the proper pinchoff voltage to make normally-off FETs. If a slight etch is needed, 10:1:1 (H_2SO_4:H_2O_2:H_2O) will probably suffice.

With improved OM or MBE epitaxial layers, the all-OM HJFET can also be tried again. Earlier we mentioned that the program ended before several metallization experiments could be done. A AuGe/Ni/Au metallization with a 3-step Au

evaporation may solve the problem of gold bridging over the oxide as well as Cr/AuGe/Au and give lower gate contact resistance. Also the metallization should be carefully tried for gates aligned both parallel and perpendicular to the (011) direction. Recall that the $NH_4OH:H_2O_2:H_2O$ mesa etch is anisotropic and the oxide protection layer will thus be slightly different for the two directions. The all-OM HJFET technology is more difficult to transfer to the ring oscillator and would require one or two more masks in the ring oscillator before the device could be made.

Finally, the gate resistance problem needs more study. It is possible that holding the Zn flow for an extra 20 minutes at the end of OM gate growth (as was done several times) actually lowers the contact resistance of AuGe/Ni Au to p^+-GaAs. This has not yet been conclusively proven and a definitive contact resistance measurement is needed.

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